Broadband Wireless Experimental System for Realtime- and Hardware in the Loop Implementation

Scandinavian workshop on testbed based wireless research

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Fraunhofer

Heinrich Hertz Institute

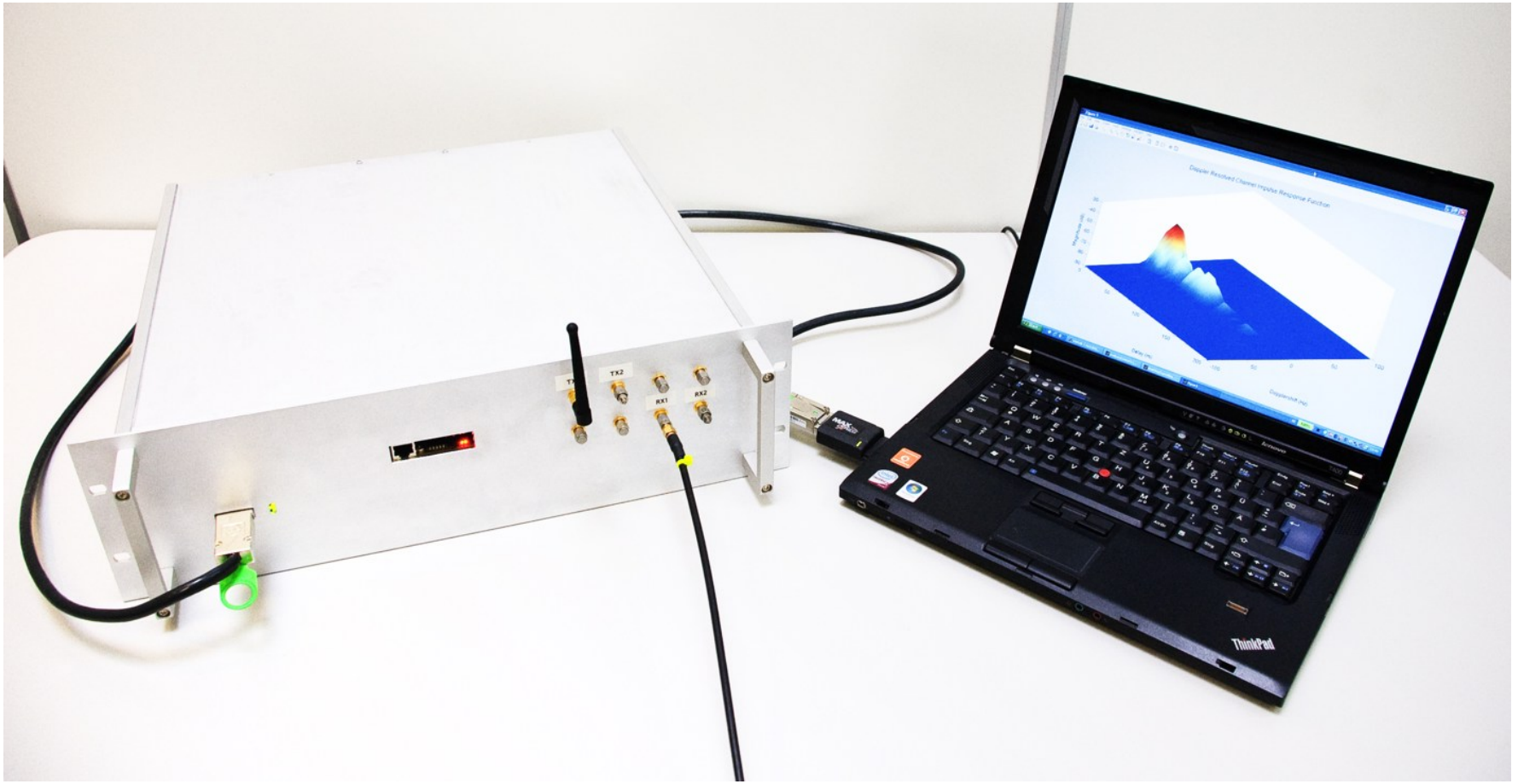
System Concept

- Flexible rapid prototyping platform for demonstrators and
  - proof of concept implementation
  - transmission scheme experiments
  - digital signal processing algorithm implementation
  - evaluation of RF-components
  - calibration methods
- Hardware construction: Sandwich structure
  - FPGA-Board consists four ALTERA Stratix III, memory, PCI-Express interface (Gidel Ltd.)
  - Main daughterboard (AD-Board): RxADCs, TxDACs, power supply, control components, Gigabit Ethernet
  - Small (40mm$\times$40mm) plug and play RF-modules: clock generators, oscillators, filters, modulators, de-modulators

System Development History

1. Generation (2005)
   - SISO
   - Tx bandwidth: 160 MHz, Rx bandwidth: 320 MHz
   - Two Stratix II FPGAs
   - PCI-X PC Board
2. Generation (2007)
   - 2x2 MIMO
   - Tx bandwidth: 250 MHz, Rx bandwidth: 500 MHz
   - Gigabit Ethernet
   - Four Stratix II FPGAs
3. Generation (2011)
   - Four Stratix III FPGAs
   - 19” Case
   - PCIe cable interface to host PC

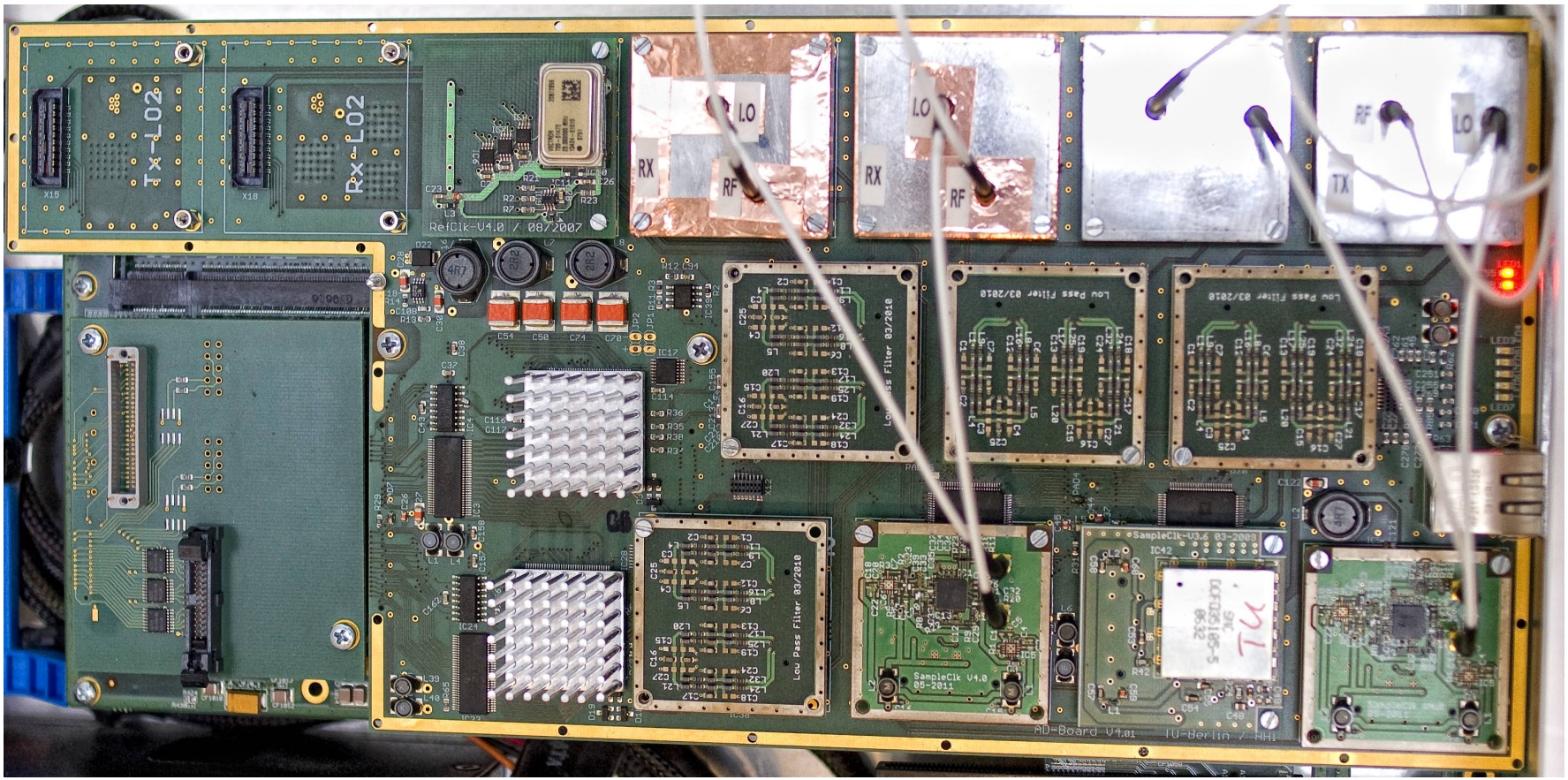
System Components



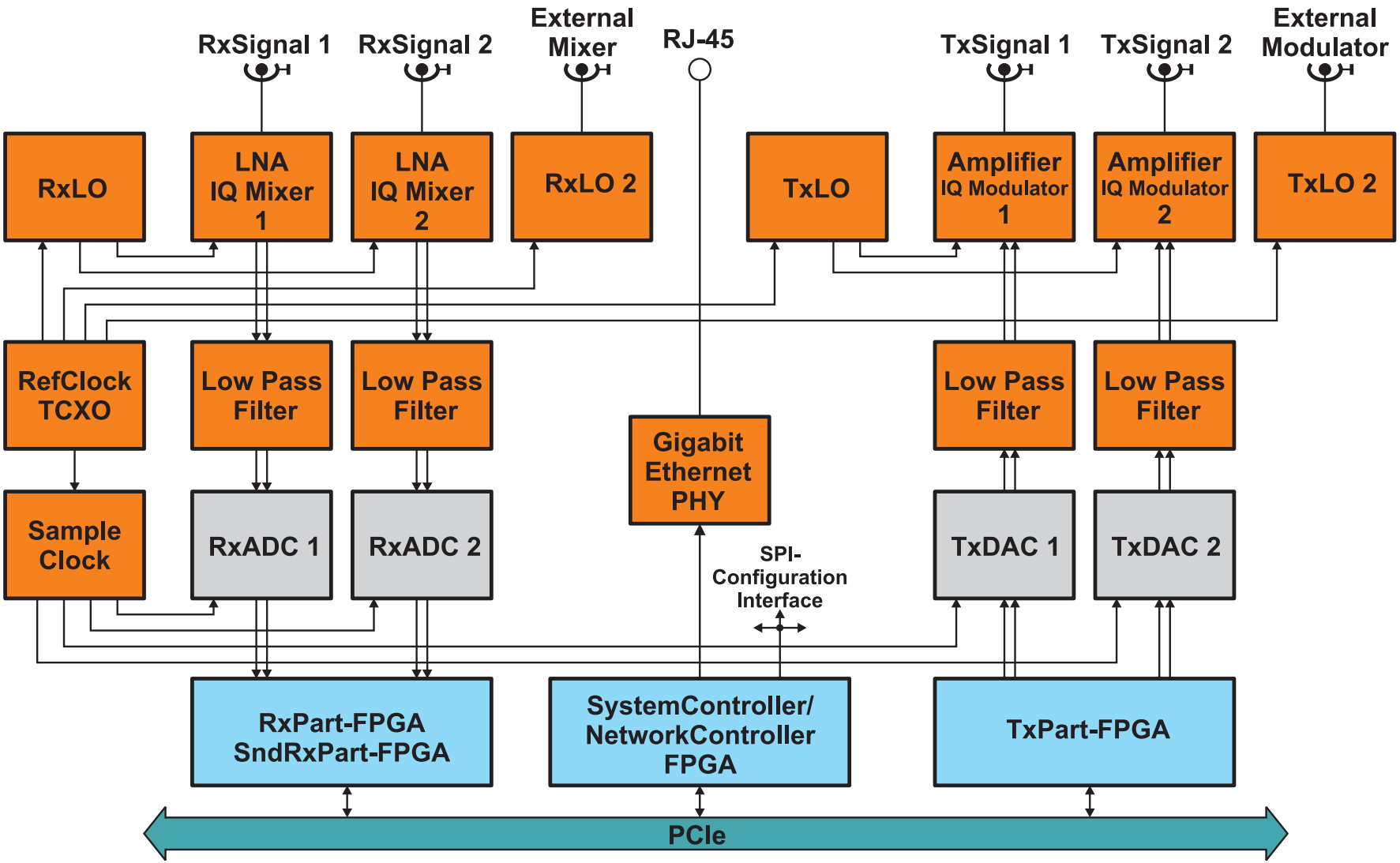
- Compact 19” case, hight: 3U, length: 400mm
- Host: Notebook or desktop PC, PCIe cable interface

Hardware Components inside the 19” Case

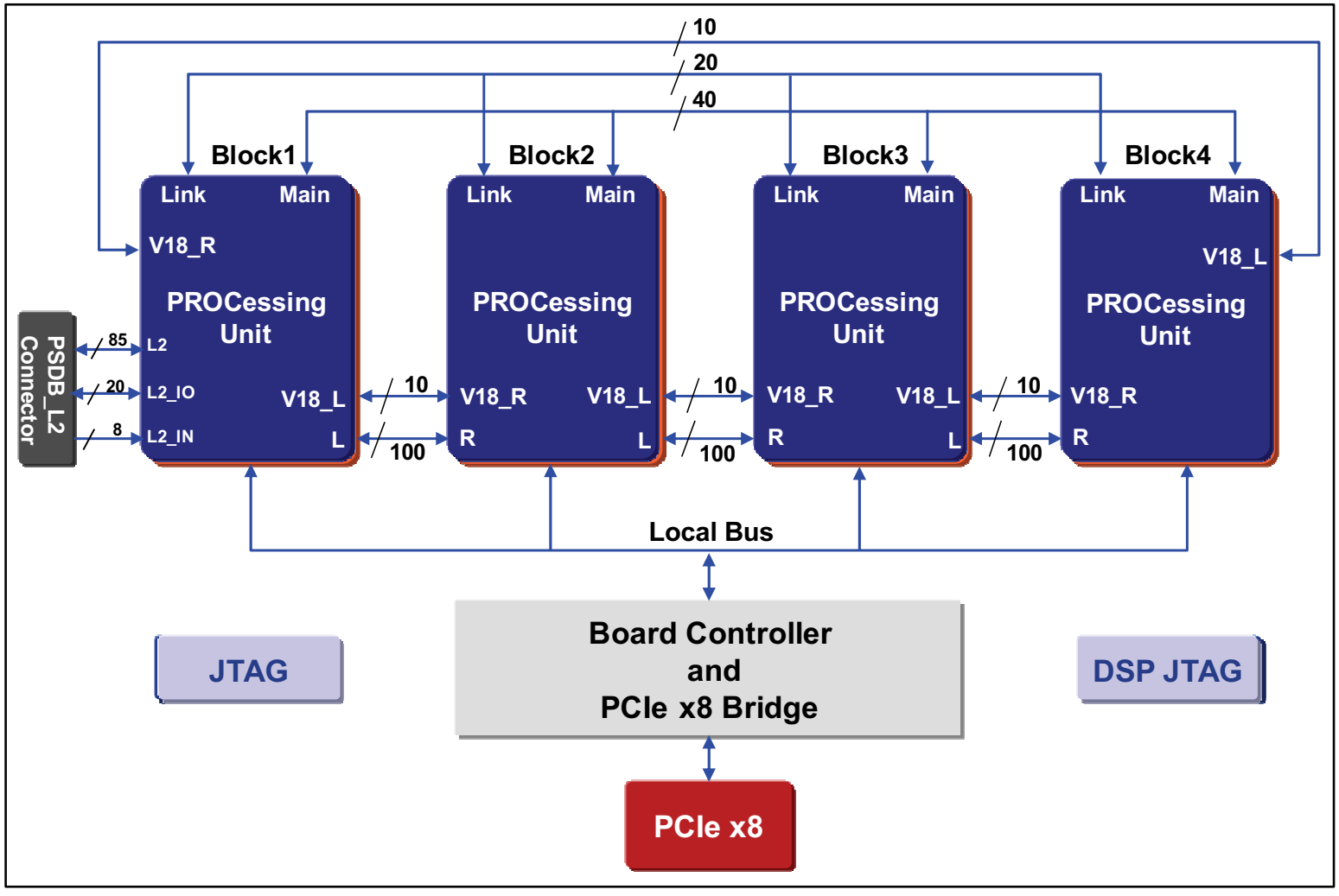
AD-Board and RF-Modules, Top View



Complete Hardware Structure



Hardware Structure - FPGA-Board, Gidel ProcStarIII

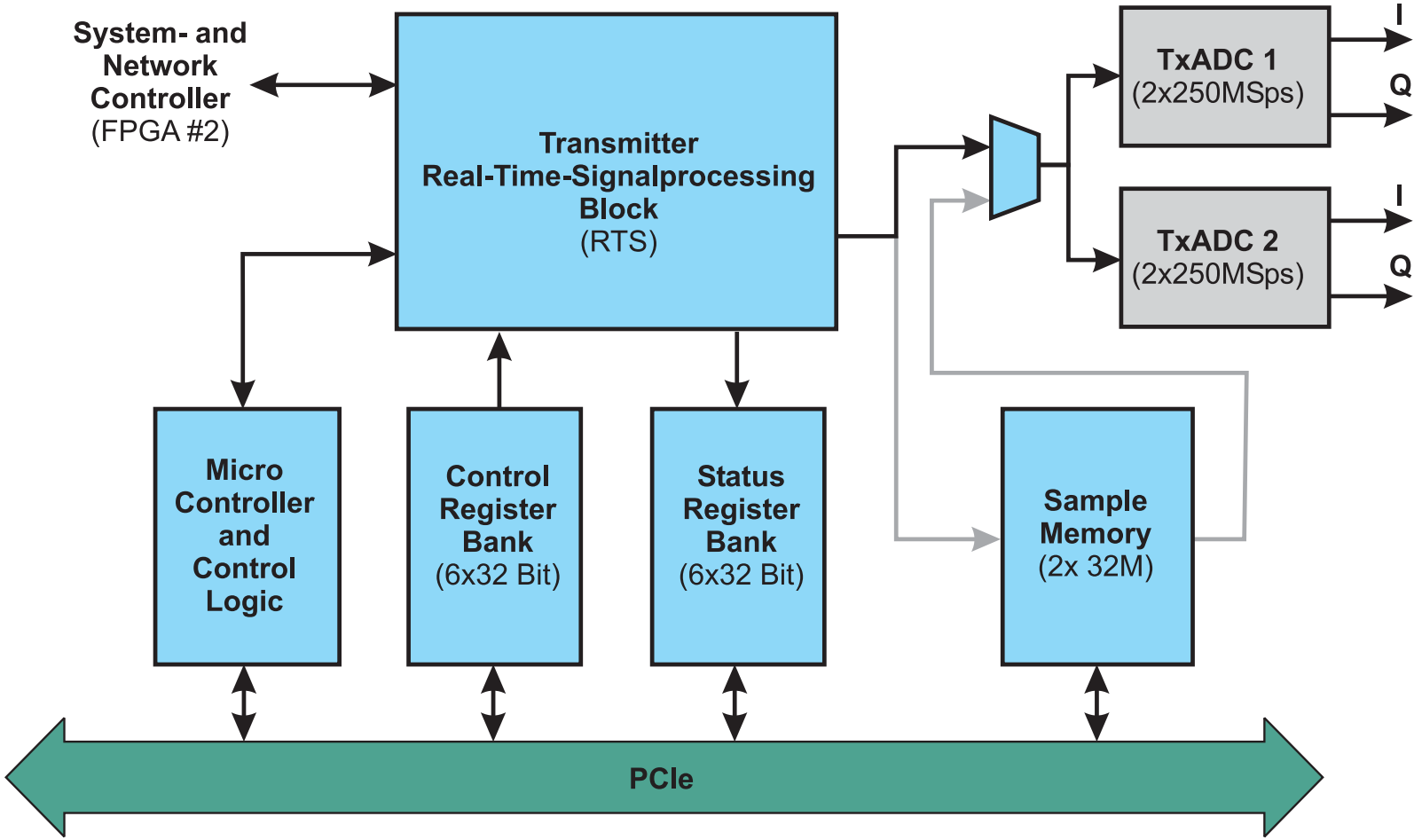


- PROCessing Units contain one Stratix III FPGA and 256 MB DDR II DRAM

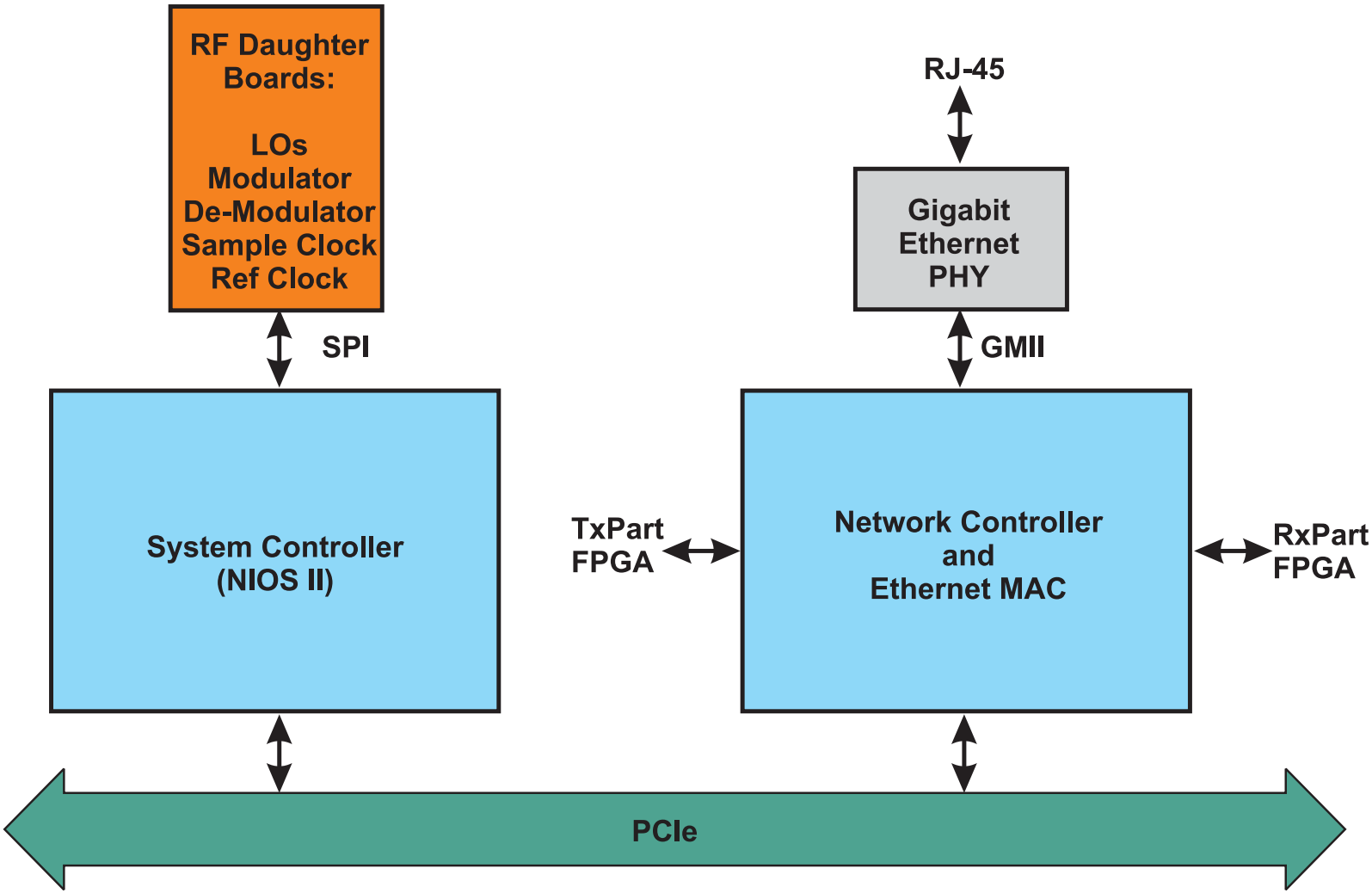
Main System Parameters

- Two IQ TxDAC
  - maximum sampling frequency = RF bandwidth: 250 MHz
  - resolution: 16 bits
- Two IQ RxADC
  - maximum sampling frequency = RF bandwidth: 500 MHz
  - resolution: 8 bits
- Processing speed
  - maximum clock frequency: $\approx$250 MHz
  - synchronous operation of large pipelined systems
  - maximum data rate / throughput: $\approx$1 Gbps
- Data interfaces: PCI-Express x4, Gigabit Ethernet
- Debugging: Signal sample memory, Logic-Analyzer interface, JTAG interface
- Operation control software: MatLab GUI and MatLab scripts

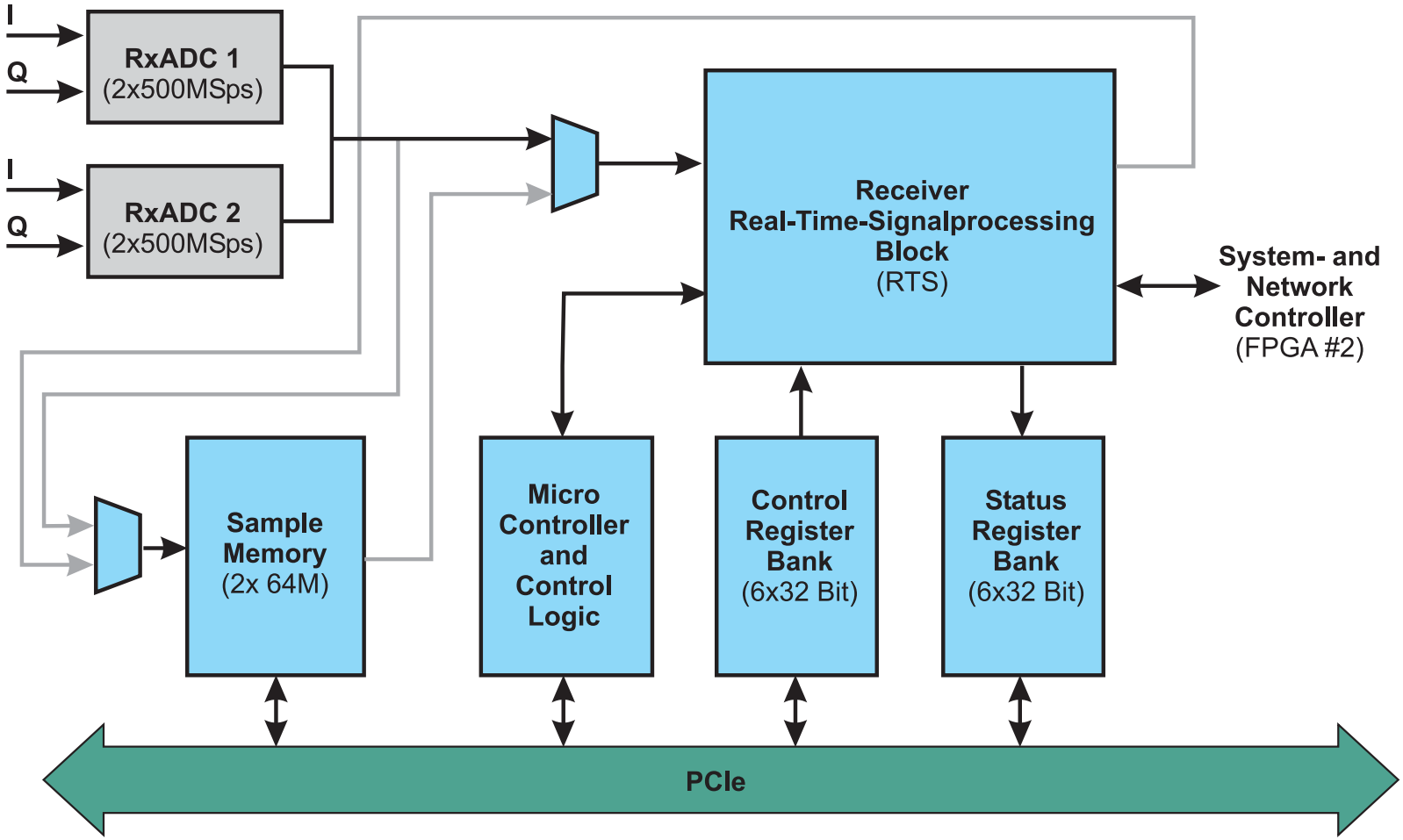
TxPart Structure (FPGA #1)



ControllerPart Structure (FPGA #2)



RxPart-Structure (FPGA #3 & 4)



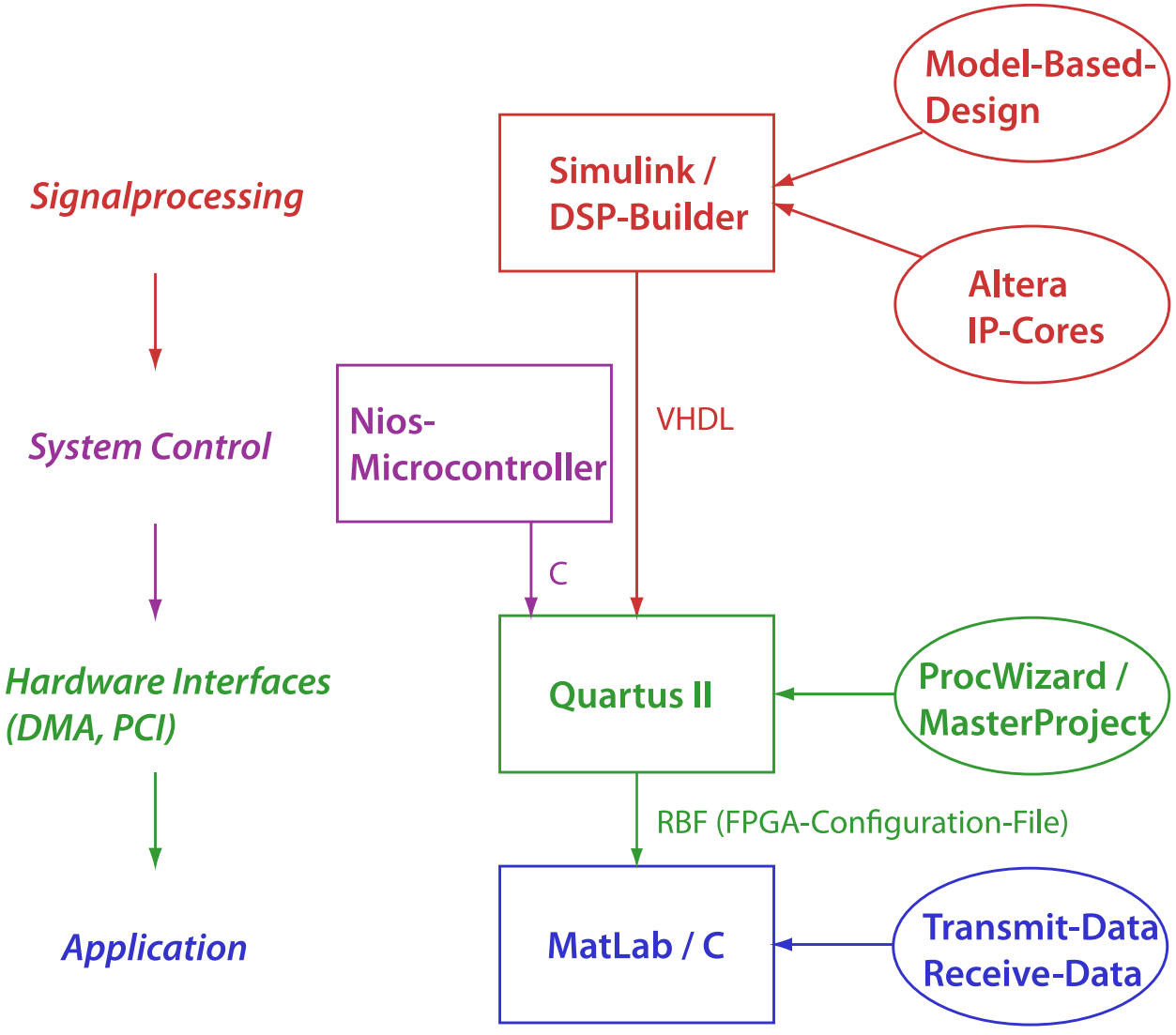
Software-Interfaces

- Complete operation software in MatLab available
- MatLab-GUI for direct access to the system resources
- Ready to use MatLab scripts for hardware-in-the-loop system development and operation available
  - only MatLab license required
- Development of dedicated MatLab GUI and scripts to control, monitoring and evaluation of implemented real time processing cores

Design Tools for Real Time Core Development

- No HDL programming required (VHDL, Verilog)
- No FPGA development tools required for hardware-in-the-loop (HIL) operation
- High level FPGA design tools for real time signal processing cores (RTS cores)
  - DSP-Builder (Altera Inc.)
  - Impulse CoDeveloper (Impulse Accelerated Technologies Inc.)
- Embedded microcontroller systems (NIOS-II, C++)
- Integration of RTS-cores as block symbol in Quartus II schematic (Altera design suite)
  - FPGA Master Projects with interfaces: RxADC / TxDAC, memory, control- and monitor registers
- Timing verification with Quartus II / TimeQuest
  - required design changes are carried out in high level design domain

Tool Chain / Design Flow



Necessary Software Tool Licenses for Real Time Core Development

- MatLab / Simulink
- Quartus II / DSP-Builder / NIOS-II Software Build Tool
- Gidel IP-Cores

Current Applications (1)

- Implementation of hardware in the loop transmission applications
  - EU-Project: SAPHYRE, synchronized and coherent operation of several devices for cellular experiments
  - Lab course „Digital Mobile Communication” at Technical University of Berlin, remote access of students to the transmission system via LAN
- Several transmission experiments at 2 GHz and 60 GHz
- 60 GHz realtime MIMO transmission with NLOS capability, cooperation with Chalmers University of Technology (ICC 2009, Dresden)
  - Space time coding, maximum ratio combinig
- OFDM realtime transceiver (IEEE 802.11a/p subset) (Project: Ko-FAS / Ko-TAG, Ministry of Economics)

Current Applications (2)

- Development and implementation of algorithms for power amplifier linearization and IQ calibration (Project: SmartRF, Ministry of Economics)
- Implementation of parallel processor systems for multiuser-detection (Project: TEROPP, Ministry of Education and Research)
- Indoor channel sounding
  - real time demonstration
  - machine to machine communication, cooperation with Johannes Kepler University Linz, Austria

Outlook

- Implementation of further real time processing cores within HHI and TU-Berlin research projects
- Development of frontend modules for further frequency domains (800 MHz, 3...6 GHz)
- Possible commercialization of the Wireless Experimental System
  - determination of market potential and requirements of possible customers
  - estimated price per device for standard FPGA size: 20 k€
  - estimated price per device for extended FPGA size: 33 k€

Today's Platform Demonstration

1. 2x2 MIMO Channelsounder
   - 250 MHz bandwidth
   - >70 dB dynamic range
2. SISO Real Time Channelsounder
   - Measurement, processing and vizualization of delay Doppler spread function
   - 7.3 measurements per second
3. OFDM Transmission (Car2Car, reduced IEEE 802.11p PHY)