

FPGA Design with VHDL

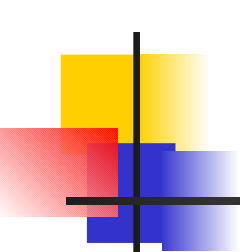
Justus-Liebig-Universität Gießen,
II. Physikalisches Institut

Ming Liu

Dr. Sören Lange

Prof. Dr. Wolfgang Kühn

ming.liu@physik.uni-giessen.de



Lecture 3

- Design Example Demo
 - VHDL Description on Designs
 - Testbench
 - Functional Simulation with Modelsim
 - Synthesis and Implementation with ISE
- About the Labs