



Compute Node Design for DAQ and Trigger Subsystem in Giessen

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Outline

- Design goals
- Current work in Giessen
 - Hardware
 - Software
- Future work

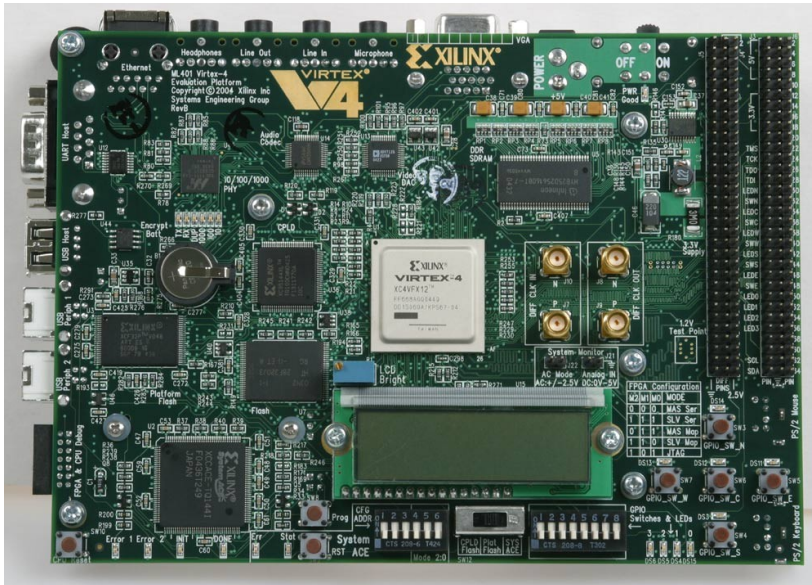


Design Goals

For compute networks and nodes in PANDA, they are expected to have:

- High computing and communication capabilities to process large amount of data.
- Highly universal, configurable and scalable platform for multiple applications.
- Convenience to be modified and upgraded in-field.

Present Work in Giessen



- Prototype design
- Based on ML403 commercial board from Xilinx.



ML403 Evaluation Board

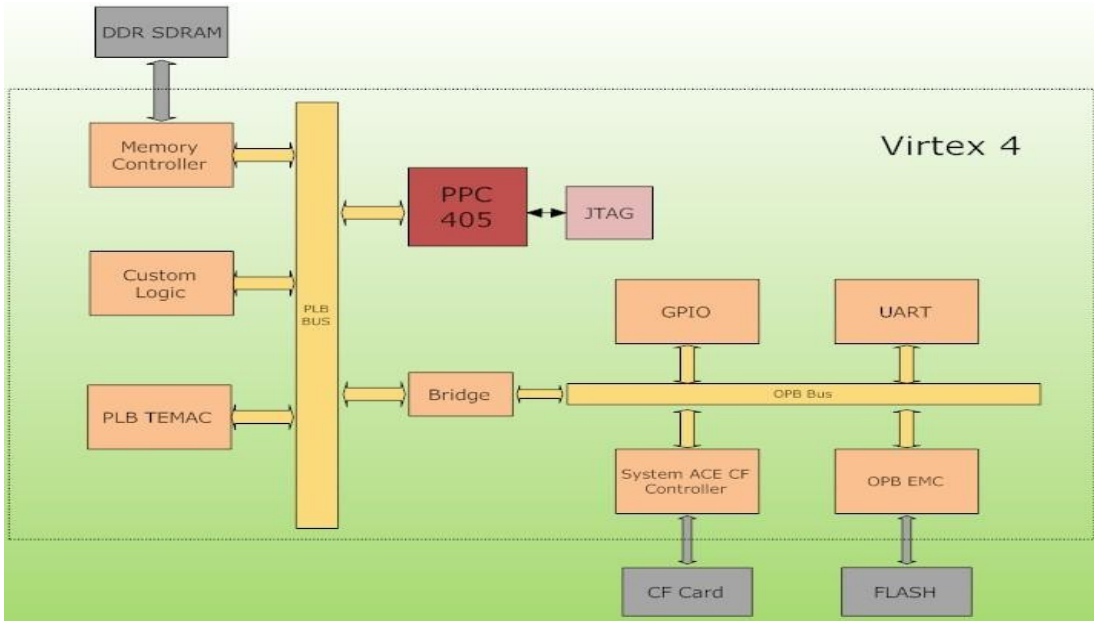
- **Xilinx Devices:**
 - Virtex 4 XC4VFX12-FF668-10 FPGA
 - 2 Audio (Microphone/Head Phone)
 - General Purpose I/O: Buttons and LEDs
 -
- **Memory:**
 - 64 MB DDR SDRAM
 - 8 Mb SRAM
 - 8 MB Linear Flash
 - 32 Mb Platform Flash
 - System ACE CF card
 - 4 Kb IIC EEPROM
- **Display:**
 - 16 x 2 Character LCD
 - DB 15 VGA Display
- **Clocks:**
 - 100 MHz Oscillator
 - 2 Clock Sockets
- **Interfaces:**
 - 10/100/1000 RJ-45 Ethernet Port
 - RS-232 Serial Port
 - JTAG
 - 3 USB Ports
 - 2 PS/2 Connectors (Keyboard/Mouse)



Virtex 4 FX FPGA

Device	Configurable Logic Blocks (CLBs) ⁽¹⁾				XtremeDSP Slices ⁽²⁾	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array ⁽³⁾ Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VSX25	64 x 40	23,040	10,240	160	128	128	2,304	4	0	N/A	N/A	N/A	9	320
XC4VSX35	96 x 40	34,560	15,360	240	192	192	3,456	8	4	N/A	N/A	N/A	11	448
XC4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	N/A	N/A	N/A	13	640
XC4VFX12	64 x 24	12,312	5,472	86	32	36	648	4	0	1	2	N/A	9	320
XC4VFX20	64 x 36	19,224	8,544	134	32	68	1,224	4	0	1	2	8	9	320
XC4VFX40	96 x 52	41,904	18,642	291	48	144	2,592	8	4	2	4	12	11	448
XC4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	16	13	576
XC4VFX100	160 x 68	94,896	42,176	659	160	376	6,768	12	8	2	4	20	15	768
XC4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	24	17	896

Hardware Platform





Hardware Platform

- Most components are inside the FPGA, such as Memory Controller, Tri-mode Ethernet, and Custom Logic.
- The programmable capability of FPGA makes it easy to modify and scale the system.
- Via custom logic design, the hardware platform could be universal for multiple applications.
- Custom logic could be designed with HDL (VHDL or Verilog) for different purposes, for instance, event-select algorithm.
- Design software:
 - EDK 8.1: high level embedded systems design.
 - ISE 8.1: logic design.
 - Modelsim 6.0: simulation.

Design in EDK

E:\work\temac_linux_proj2\system.xmp - [System Assembly View1]

Hardware Software Device Configuration Debug Simulation Window Help

Filter: ☒ Bus Interface ☐ Ports ☐ Addresses ☒ Connection Filters

Name	Bus Connection	Direction	IP Type	IP Version
ppc405_0			ppc405_virtex4	1.01.a
plb			plb_v34	1.02.a
opb			opb_v20	1.10.c
plb2opb			plb2opb_bridge	1.01.a
itagppc_0			itagppc_cntrl	2.00.a
RS232_Uart			opb_uart16550	1.00.d
SysACE_CompactFlash			opb_sysace	1.00.c
DDR_SDRAM_64Mx32			plb_ddr	1.11.a
plb_bram_if_cntrl_1			plb_bram_if_cntrl	1.00.b
opb_intc_0			opb_intc	1.00.c
plb_temac_0			plb_temac	2.00.a
MSPLB	plb			
V4EMACSRC	plb_temac_0_V...			
hard_temac_0			hard_temac	1.00.a
V4EMACDST0	plb_temac_0_V...			
V4EMACDST1	No Connection			
FLASH_2Mx32			opb_emc	2.00.a
opb_fifo_0			opb_fifo	1.00.c
plb_fifo_0			plb_fifo	1.00.b
reset_block			proc_sys_reset	1.00.a
plb_bram_if_cntrl_1_bram			bram_block	1.00.a
sysclk_inv			util_vector_logic	1.00.a
clk90_inv			util_vector_logic	1.00.a
ddr_clk90_inv			util_vector_logic	1.00.a
dcm_0			dcm_module	1.00.a
dcm_1			dcm_module	1.00.a
dcm_3			dcm_module	1.00.a
invGate_0			util_reduced_logic	1.00.a
FLASH_2Mx32_util_bus_split_0			util_bus_split	1.00.a

Legend

☐ Master ☐ Slave ☐ Master/Slave Target Initiator Connected Unconnected

☒ System Assembly...

c:\download.cmd
e: etc/fast_runtime.opt
gen.ut

Design in EDK

io - E:\work\temac_linux_proj2\system.xmp - [System Assembly View1]

Hardware Software Device Configuration Debug Simulation Window Help

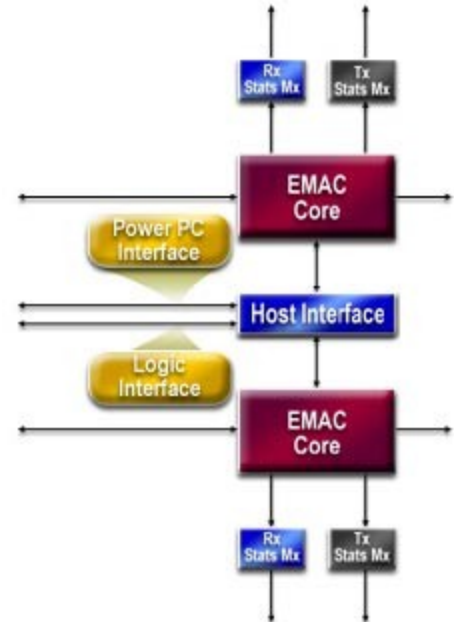
Filters
☐ Bus Interface ☐ Ports ☒ Addresses

Instance	Name	Address	Base Address	High Address	Size	Lock	ICache	DCache	Bus Connection
plb2opb	SPLB	RNG3			U	☐			plb
plb2opb	SPLB	RNG2			U	☐			plb
plb2opb	SPLB	RNG1	0x40000000	0x7fffffff	1G	☐			plb
plb2opb	SPLB	RNG0	0x20000000	0x3fffffff	512M	☐			plb
DDR_SDRAM_64Mx32	SPLB	MEM0	0x00000000	0x03ffffff	64M	☐	☒	☒	plb
DDR_SDRAM_64Mx32	SPLB	ECC			U	☐			plb
plb_bram_if_cntlr_1	SPLB	c_baseaddr:c_highaddr	0xffff0000	0xffffffff	16K	☐	☐	☐	plb
plb_fifo_0	SPLB		0xc4000000	0xc40fffff	64K	☐			plb
FLASH_2Mx32	SOPB	MEM0	0x22000000	0x227fffff	8M	☐	☐	☐	opb
opb_fifo_0	SOPB		0x7d400000	0x7d40ffff	64K	☐			opb
SysACE_CompactFlash	SOPB		0x41800000	0x4180ffff	64K	☐			opb
opb_intc_0	SOPB		0x41200000	0x4120ffff	64K	☐			opb
RS232_Uart	SOPB		0x40400000	0x4040ffff	64K	☐			opb
plb2opb	SDCR	DCR			U	☐			No Connection
plb	SDCR				U	☐			No Connection
plb_temac_0	MSPLB		0x81200000	0x8120ffff	64K	☐			plb
ppc405_0	MDCR	IDCR			U	☐			No Connection
opb					U	☐			

System Assembly...

Tri-mode Ethernet

- 2 Tri-mode Ethernet MACs in V4FX12.
- 10/100/1000 Mbps modes. (1000 Mbps is most interesting for us.)
- Gbit Ethernet provides guaranteed communication performance for interconnected networks.





Flash Memory

- FPGA configuration data and operating system image are both stored in flash memory chips.
- The hardware platform could be updated by this method: 1. power on and boot the system. 2. update the configuration data in flash. 3. reboot the system. (talk about it later in detail)
- Also the operating system image.

Software

- An open source Linux 2.6 runs on PPC 405.
- Totally free and well maintained by many people around the world.
- Many device drivers and other resources from Internet.
- Powerful network support, suitable for our case.





Software

With the OS support,

- the hardware and software platform could be universal for multiple uses via different application programs.
- physicists could write their own application programs with high level programming languages, such as C and C++, without the knowledge of circuit design.
- applications could be more portable among different architectures.



Kernel Compilation

- Getting the kernel sources
 - www.kernel.org
 - www.penguinppc.org
- Configuring the kernel
 - ARCH := ppc
 - Select the features which are to be included in the kernel.
- Building a PowerPC cross-compile toolchain
 - Cross-compiler: powerpc-405-linux-gnu-gcc
- Then, compiling...



Network File System

- Generating the root file system
 - busybox
- Mounting the root file system via NFS
 - “Diskless” booting and the on-board flash memory space could be saved.
 - The file system could be easily changed through PC operations, without frequently copying files into CF card or flash chips.
 - Convenient especially for in-field file modification.

System Upgrading

- The OS kernel image and the hardware configuration data are both stored in the flash chips on board.
- After the booting of Linux, the flash memory could be addressed via its device driver. Then the configuration data and kernel image could be upgraded in Linux.
- Reboot the system and hence the updated hardware and OS begin working.
- Operated remotely and need no download cable.



Current Progress

- Now Linux 2.6 is running on the ML403 platform, with Gbit Enet data transfer, NFS, reserved memory for buffering incoming data, and many other features supported.
- Host (PC) and client (board) transceiving application programs have been realized to transfer packets along the dataflow with UDP protocol successfully.



Future work

- Measuring the detailed latency and throughput parameters of the network
- Well-designed transceiving programs for Enet data transfer
- Custom logic design for specific algorithm
- Many things to do...

Thank You!