HW Implementation of the Inner Track Reconstruction

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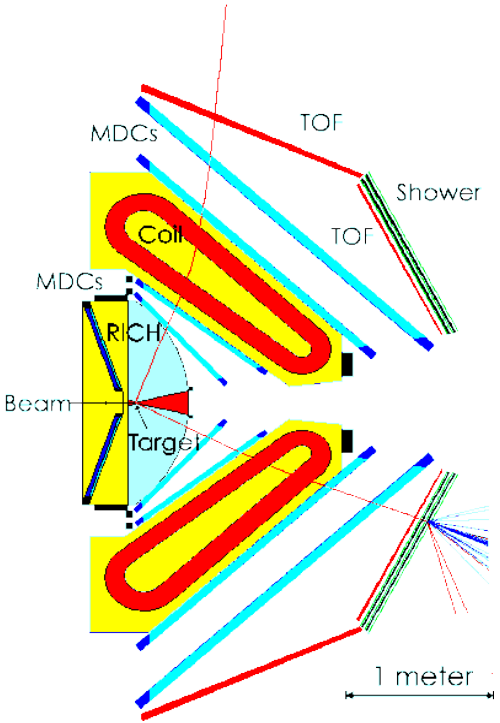
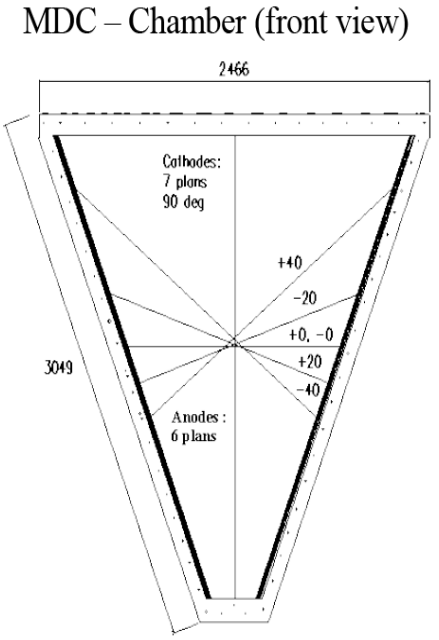
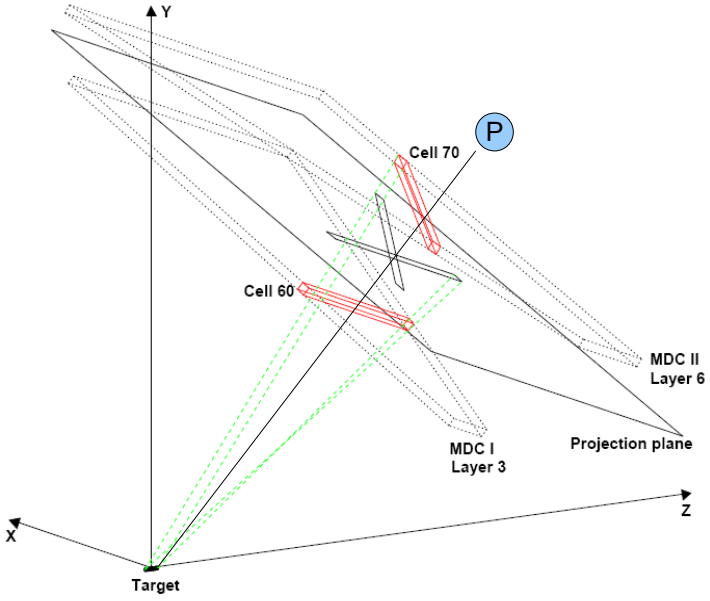
Tracking in MDC



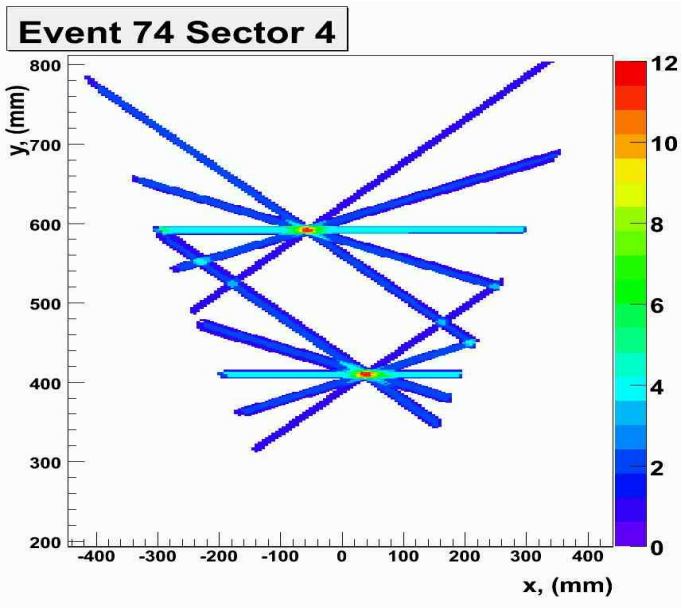
- 4 MDCs
- Particles' tracks bended in the magnetic area
- Straight line tracks from target to MDC II, and from MDC III to MDC IV
- Currently focusing on the tracks from target to MDC II

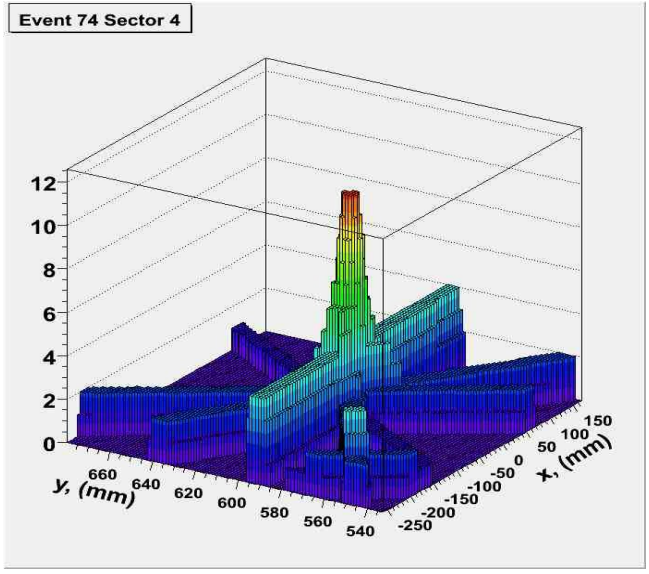
Dubna Tracking Principle





Dubna Tracking Principle





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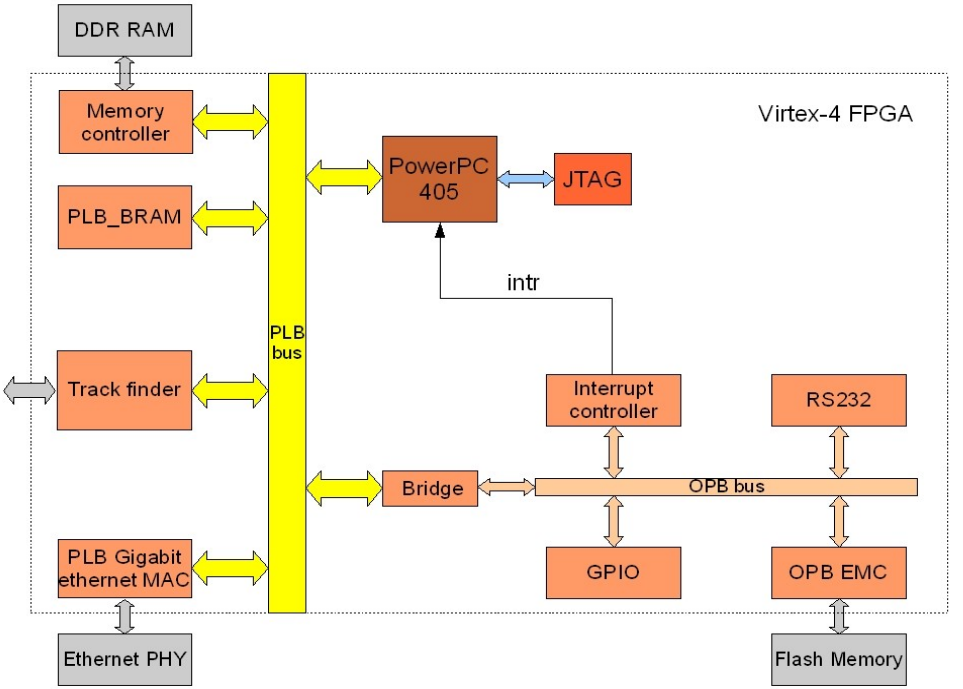
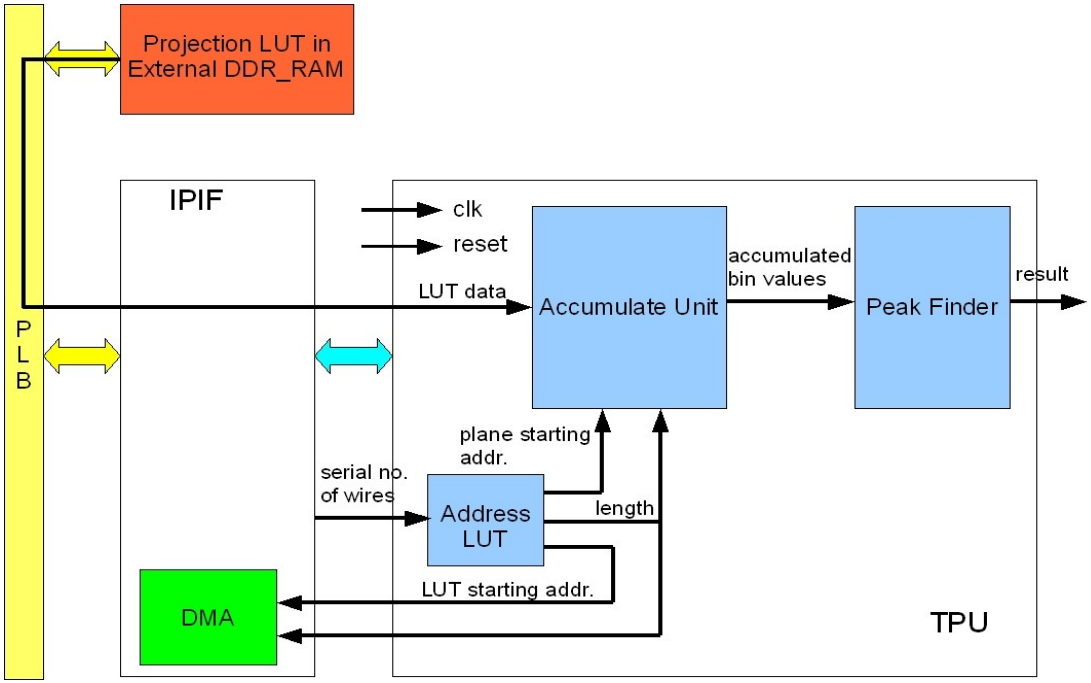
Daniel Kirschner

Geydar Agakishiev

System Architecture



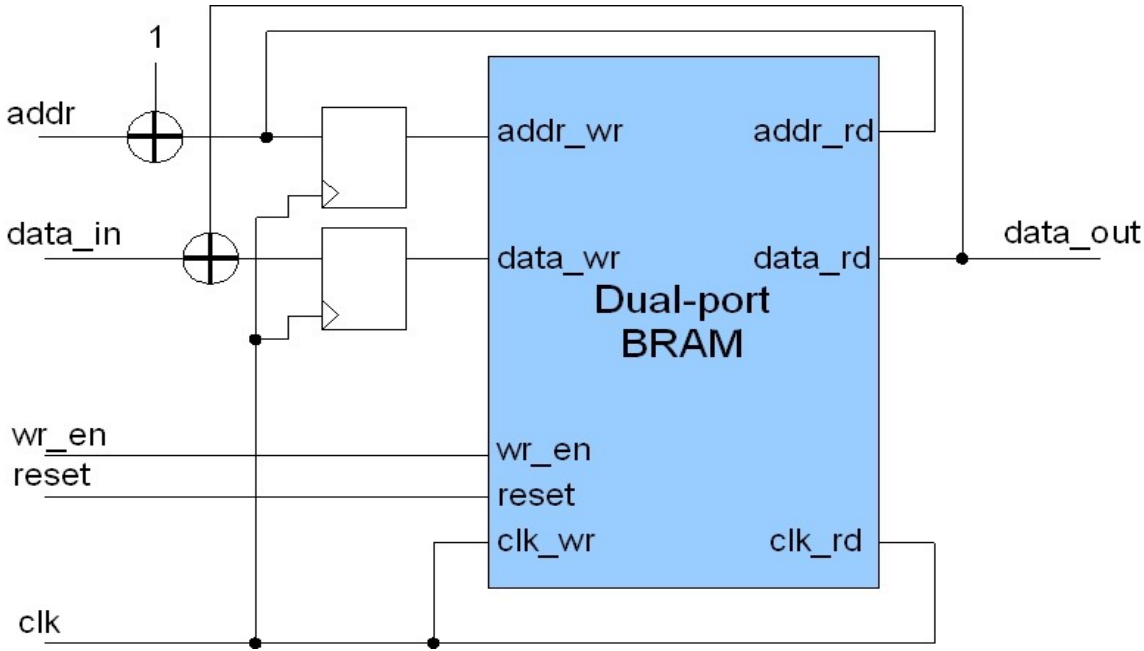
TPU Design


Projection LUT in
External DDR_RAM
IPIF
clk
reset
LUT data
Accumulate Unit
accumulated
bin values
Peak Finder
result
P
L
B
plane starting
addr.
serial no.
of wires
Address
LUT
length
LUT starting addr.
DMA
TPU

LUTs

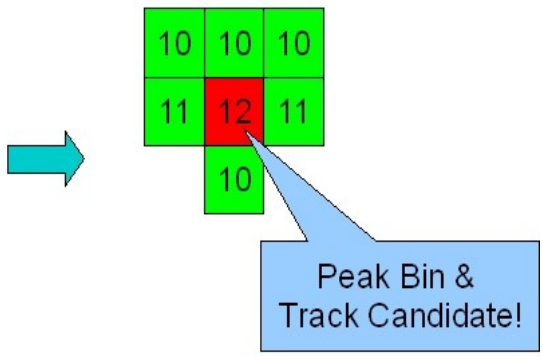
- Two LUTs: projection LUT & address LUT
- Projection LUT provides the projection mappings for all the wires.
- Address LUT stores the address info. for each wire:
  - Plane starting addr.
  - LUT starting addr.
  - length

Accumulate Unit



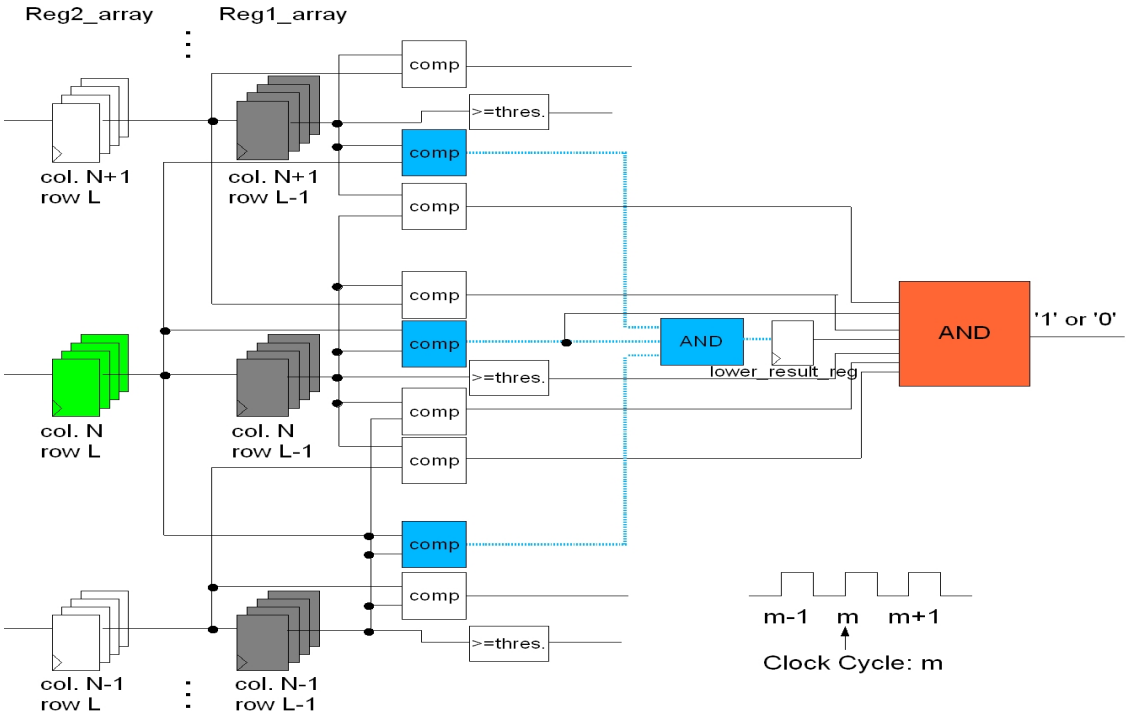
Peak Finder

0	2	0	2	0	0	0	2	0	2	0
0	0	4	4	10	10	10	4	4	0	0
4	4	7	9	11	12	11	9	7	4	4
4	4	4	4	9	10	9	4	4	4	4
0	0	2	4	0	0	0	2	4	0	0
0	2	0	0	0	0	0	0	0	2	0

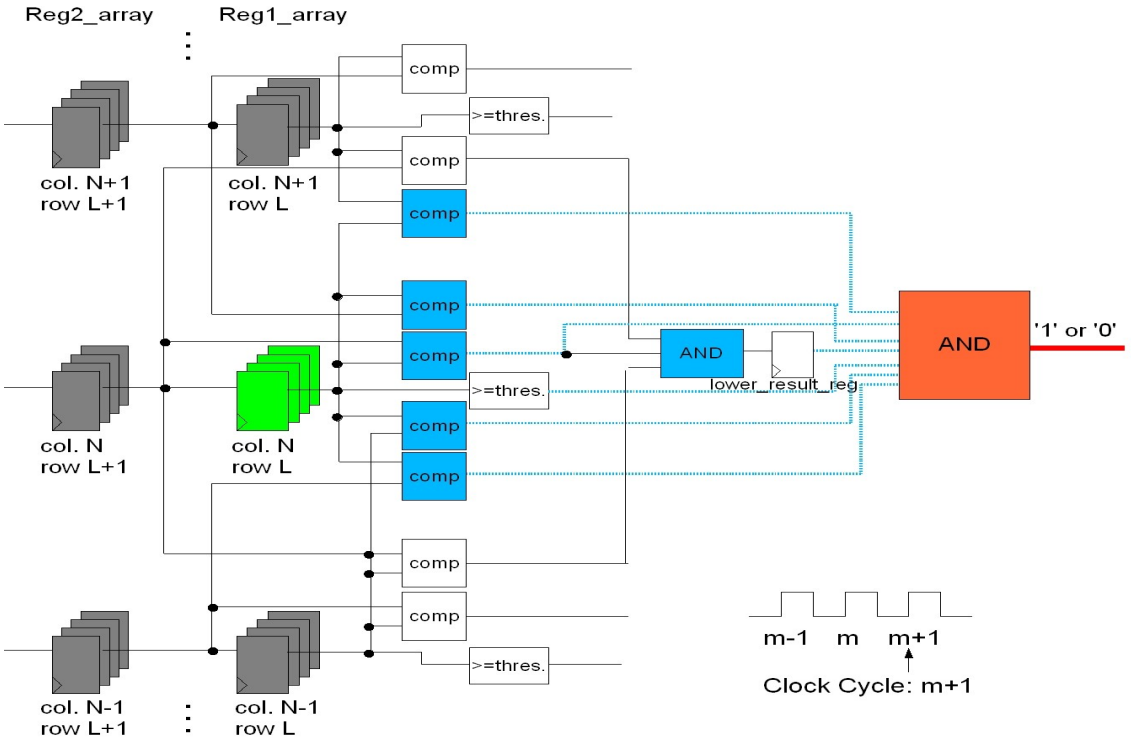


Threshold = 10

Pipelined arch. of Peak Finder



Pipelined arch. of Peak Finder



Implementation Results

Resources	TPU	compute node platform	PLB-IPIF	system with TPU (sum)
4-input LUTs	4755 out of 50560 (9.4%)	8531 out of 50560 (16.9%)	2900 out of 50560 (5.7%)	21817 out of 50560 (43.2%)
Slice Flip-Flops	2744 out of 50560 (5.4%)	5724 out of 50560 (11.3%)	1640 out of 50560 (3.2%)	10108 out of 50560 (20%)
Block RAMs	24 out of 232 (10.3%)	18 out of 232 (7.8%)	0	42 out of 232 (18.1%)
DSP Slices	0	8 out of 128 (6.3%)	0	8 out of 128 (6.3%)

- Resource utilization is acceptable.
- Timing limitation: 125 Mhz.
- We choose 100 Mhz, matching the speed of PLB.

Summary

- Basic principle of the inner track reconstruction was implemented in Xilinx FPGA fabric.
- Working as a processing engine in compute nodes, the TPU works to find out track candidates.
- It is feasible to implement the entire system in FPGA.