Embedded Implementation of Track Reconstruction Algorithm

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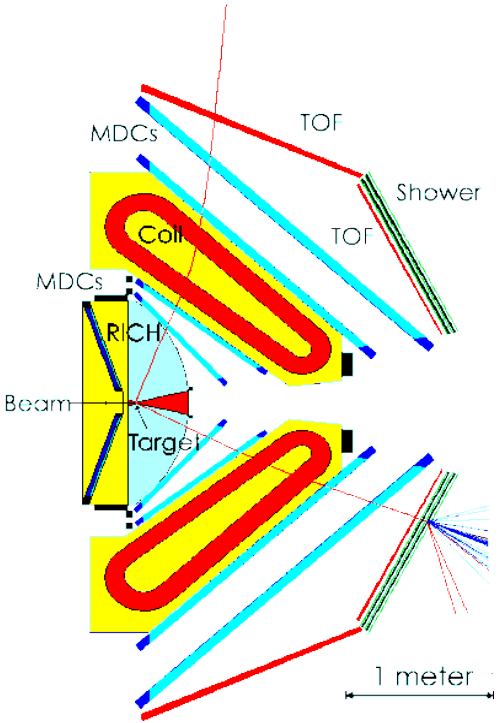
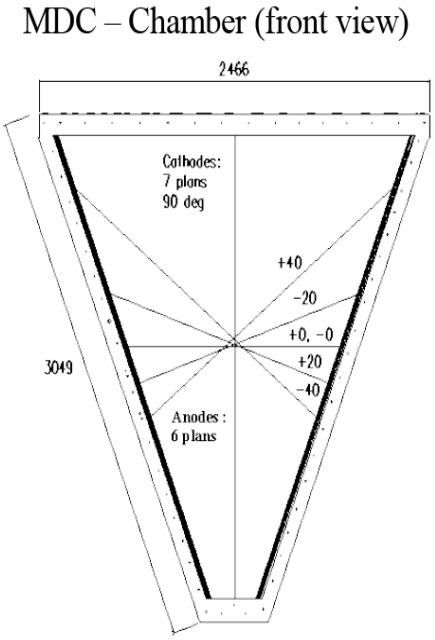
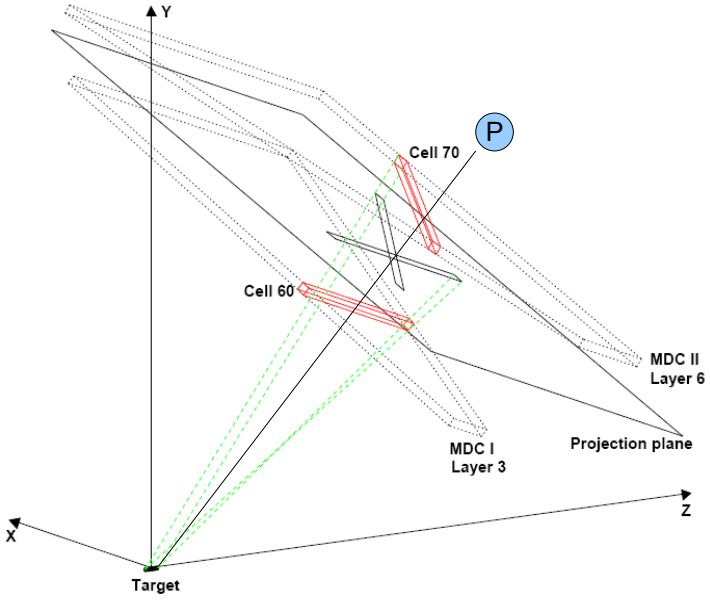
Tracking in MDC



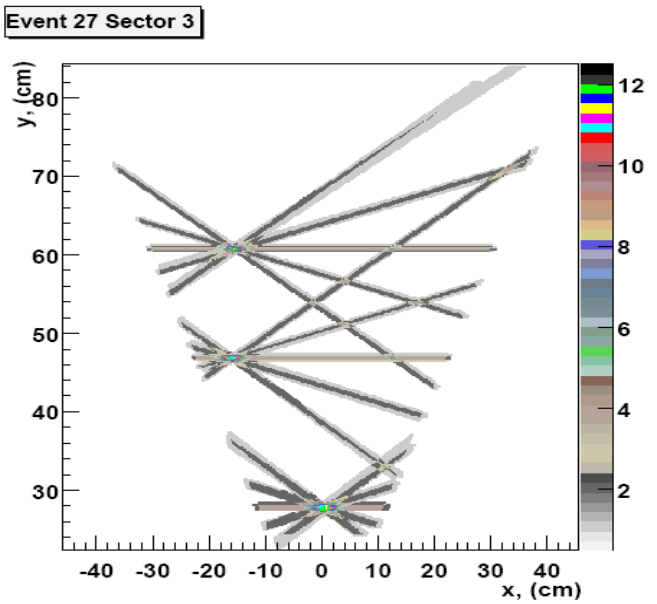
- 4 MDCs
- Particles' tracks bended in the magnetic area
- Straight line tracks from target to MDC II, and from MDC III to MDC IV
- Currently focusing on the tracks from target to MDC II

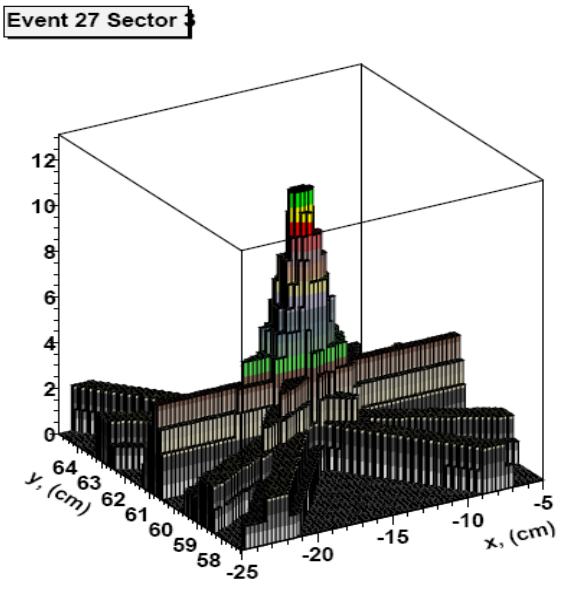
Dubna Tracking Principle





Dubna Tracking Principle





Special thanks to: Vladimir Pechenov

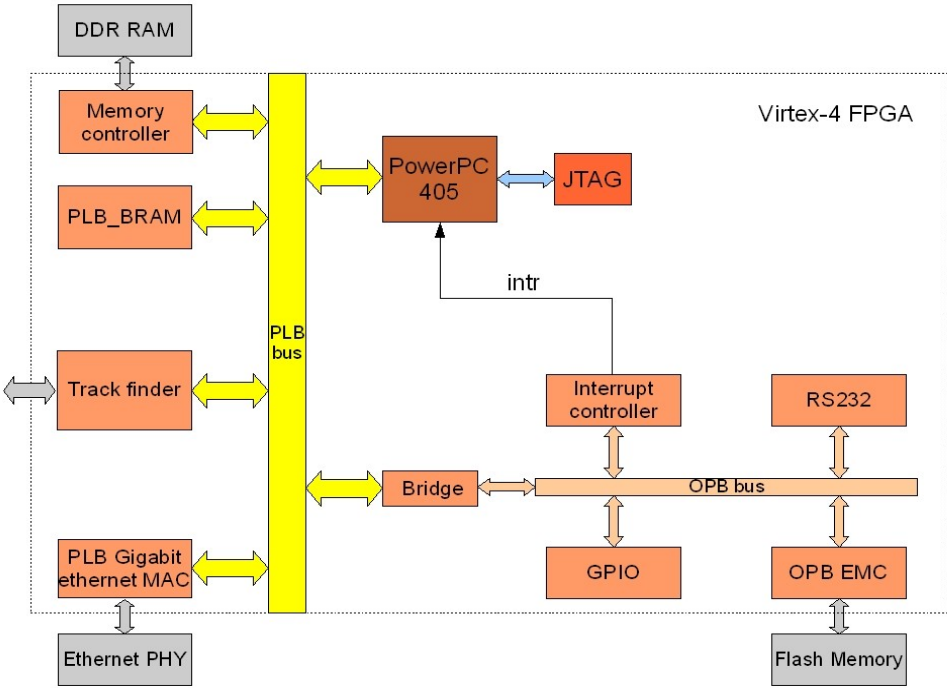
Daniel Kirschner

Geydar Agakishiev

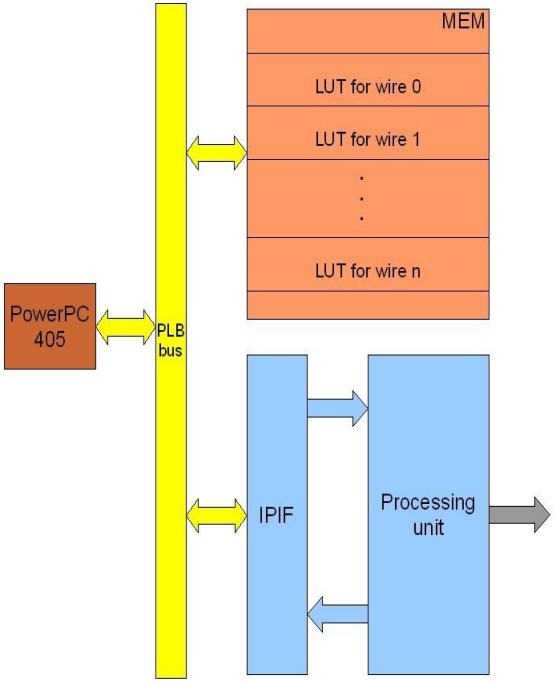
Algorithm Implementation

- Previously implemented as software
- Could be (perhaps partly) moved to on-line hardware processing to shrink the offline processing time and save storage space
- Modern FPGA techniques suitable for parallel and pipelined architecture to achieve high performance
- Integrated in CN as a computing engine module

System Architecture

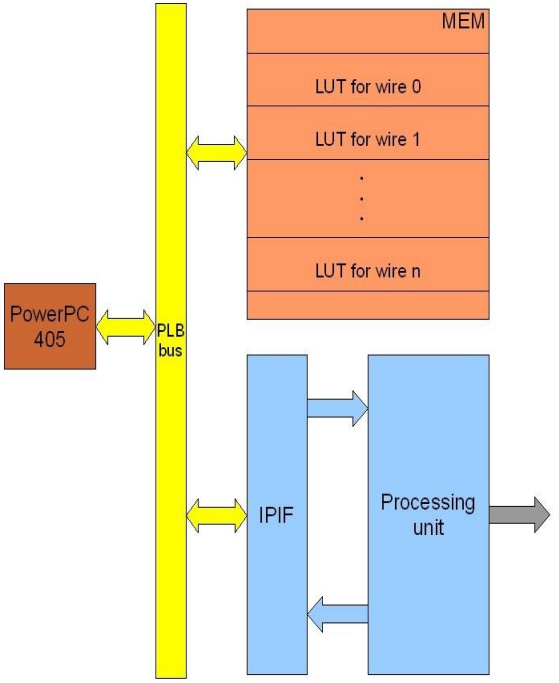


Working Mechanism



Motherbd No.,
TDC No.,
SAM No.,
...

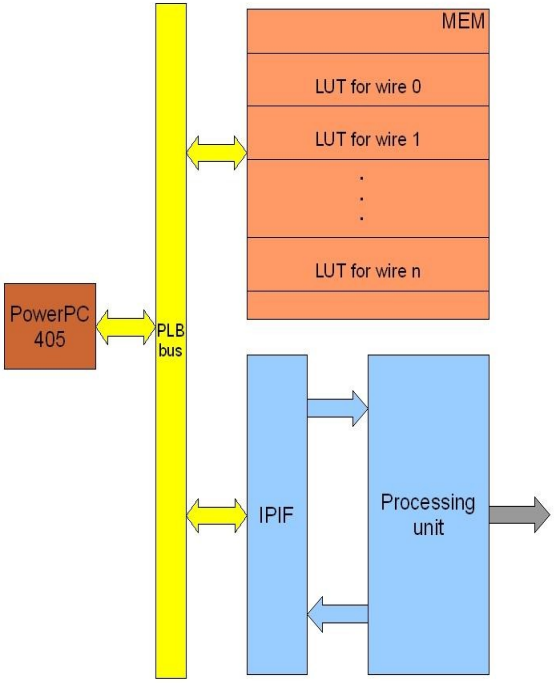
Working Mechanism



Motherbd No.,
TDC No.,
SAM No.,
...

LUT → Fired wire No.

Working Mechanism

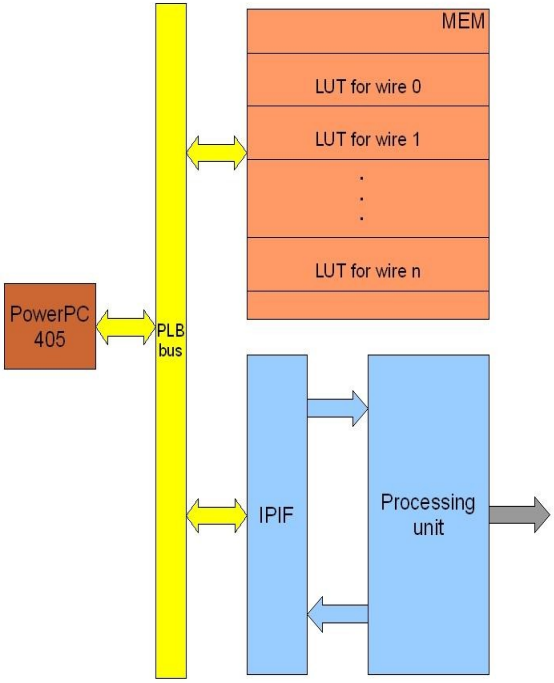


Motherbd No.,
TDC No.,
SAM No.,
...

LUT → Fired wire No. LUT →

Fired cell No.
In the
projection
plane

Working Mechanism



Motherbd No.,
TDC No.,
SAM No.,
...

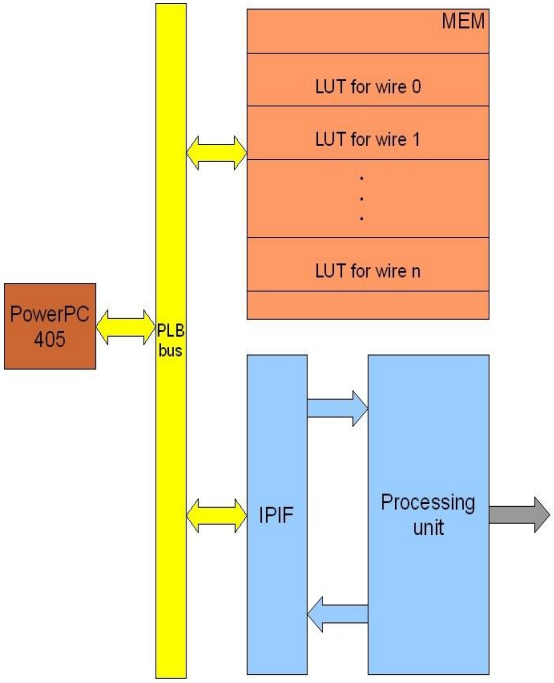
LUT → Fired wire No. LUT → Fired cell No. In the projection plane

1st fired wire

1	1	1	1	1	1	1	1

e.g. Threshold = 3

Working Mechanism



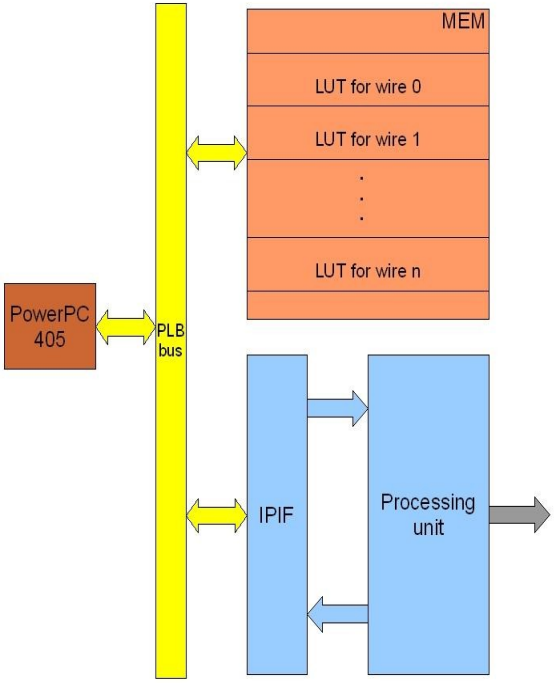
Motherbd No.,
TDC No.,
SAM No.,
...

LUT → Fired wire No. → LUT → Fired cell No. In the projection plane

								1
							1	
						1		
1st fired wire	1	1	1	1	2	1	1	1
				1				
			1					
		1						
2nd fired wire	1							

e.g. Threshold = 3

Working Mechanism



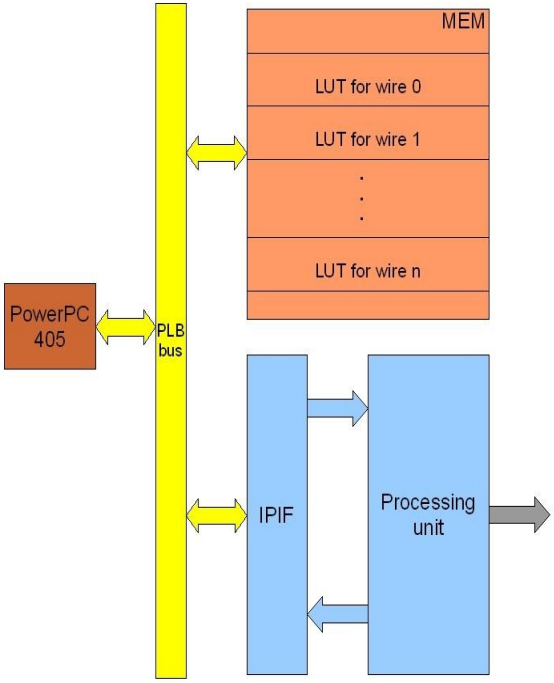
Motherbd No.,
TDC No.,
SAM No.,
...

LUT → Fired wire No. LUT → Fired cell No. In the projection plane

3rd fired wire		1						1
			1				1	
				1		1		
1st fired wire	1	1	1	1	3	1	1	1
				1		1		
			1				1	
		1						1
2nd fired wire	1							

e.g. Threshold = 3

Working Mechanism



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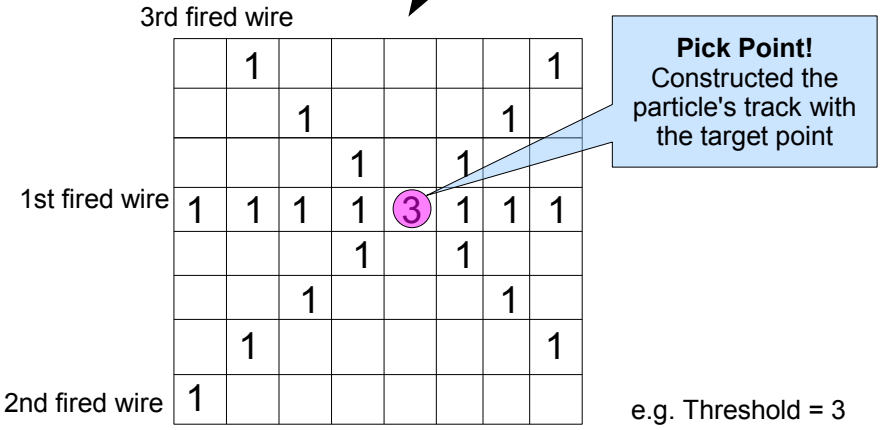
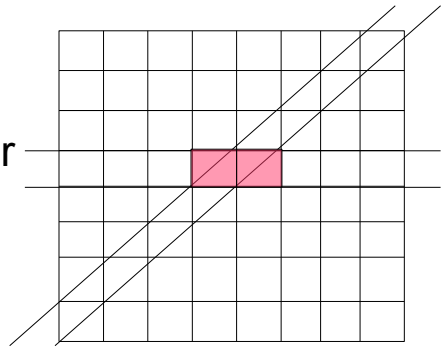


Current Status

- A demo processing unit was designed.
  - pipelined
  - 64-bit datapath width
  - Works as a PLB peripheral
  - Runs at the same clock frequency as PLB (100MHz)
- Simulation was done for functional verification in Modelsim.
- Emulation was executed on ML405, with standalone application programs.

Future Work



So much work to do in the future...

- Deep study in the algorithm and consideration for inplementation.
  - e.g. the case of multiple pick cells were chosen for a single particle track.
- To parallelize the algorithm for processing the whole projection plane in several FPGAs to achieve high performance.
- To relocate the processing unit as an Auxiliary Processing Unit (APU) , rather than as a PLB peripheral.