



# System-on-an-FPGA Design for Real-time Particle Track Recognition and Reconstruction in Physics Experiments

Ming Liu<sup>†‡</sup>, Wolfgang Kuehn<sup>†</sup>, Zhonghai Lu<sup>‡</sup>, Axel Jantsch<sup>‡</sup>



II. Experimental Physics Institute,  
Justus-Liebig-University in Giessen, Germany



Dept. of Electronic, Computer and Software Systems,  
Royal Institute of Technology, Stockholm, Sweden

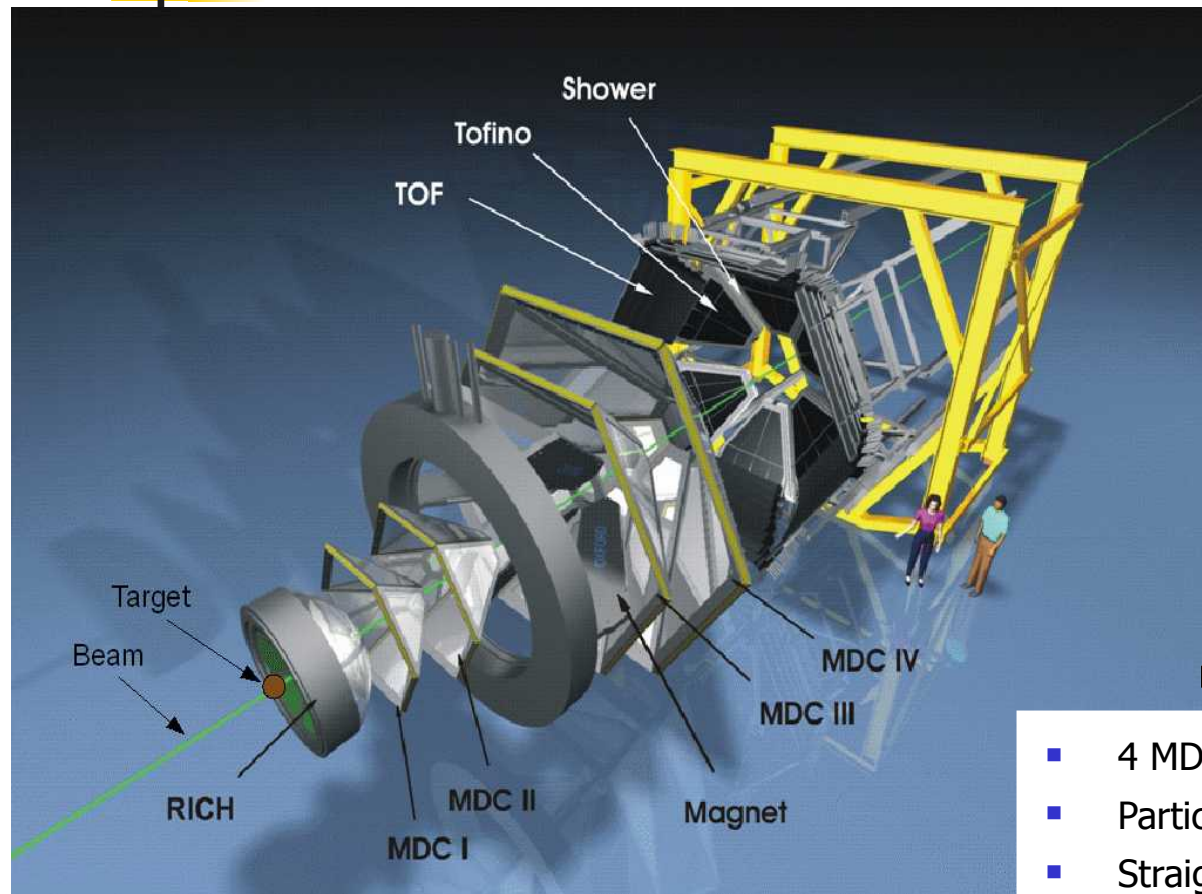


# Outline

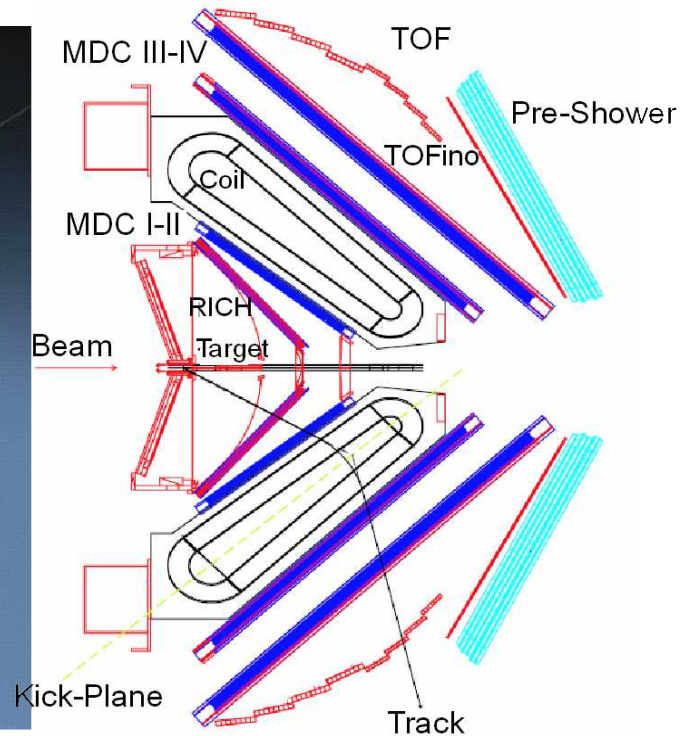
---

- Background & algorithm description
- Tracking Processing Unit (TPU) design on FPGA
- Experimental results

# Detector System for Particle Collisions

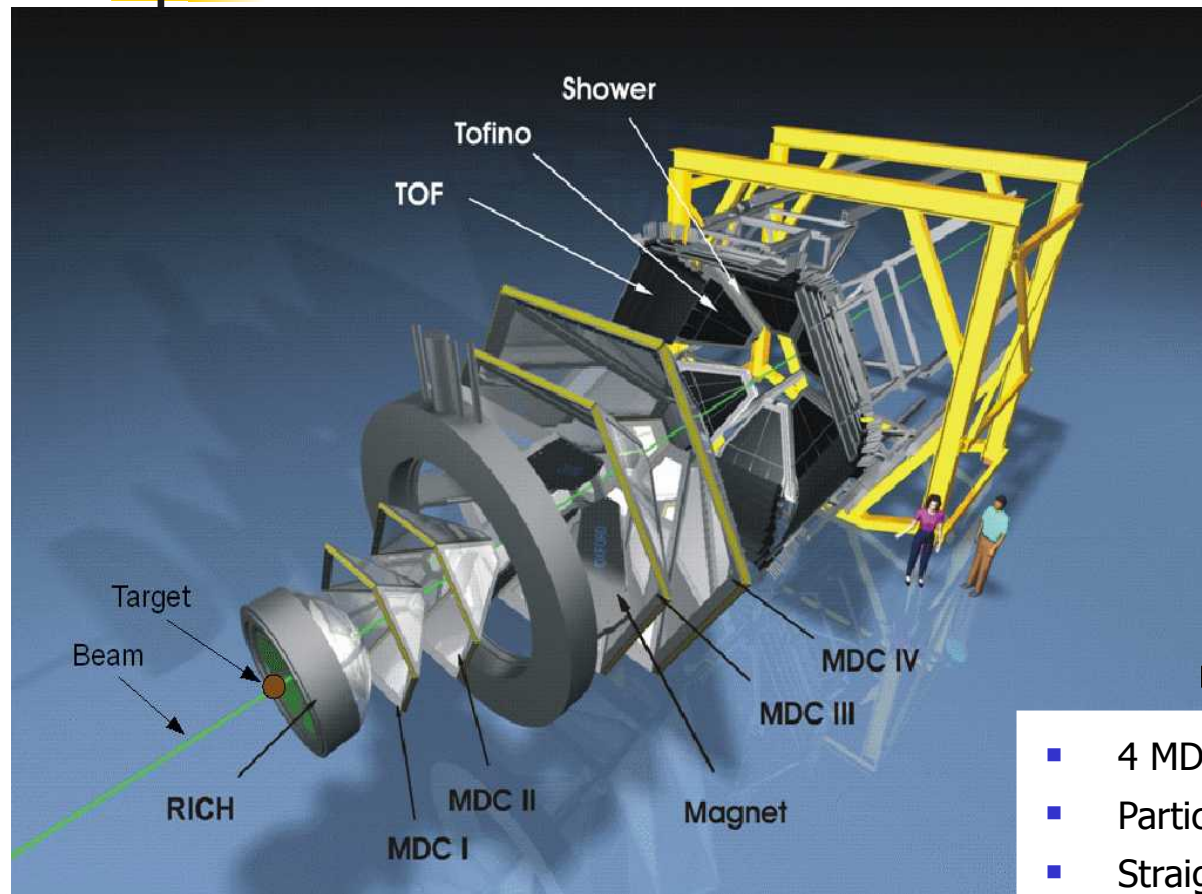


HADES detector system

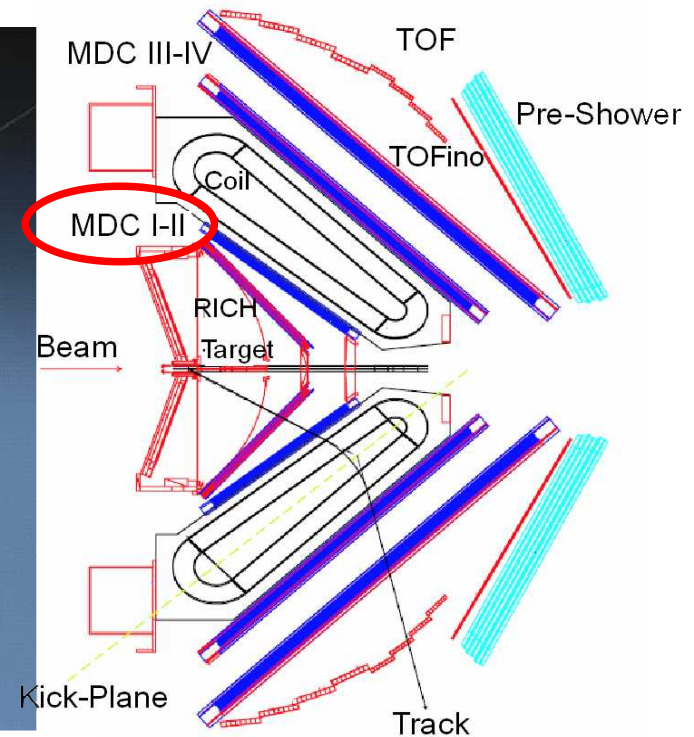


- 4 MDC detectors (2 before & 2 after the coil)
- Particle tracks bended in the magnetic area
- Straight line tracks from target to MDC II, and from MDC III to MDC IV
- Currently focusing on the inner part, due to a similar principle

# Detector System for Particle Collisions



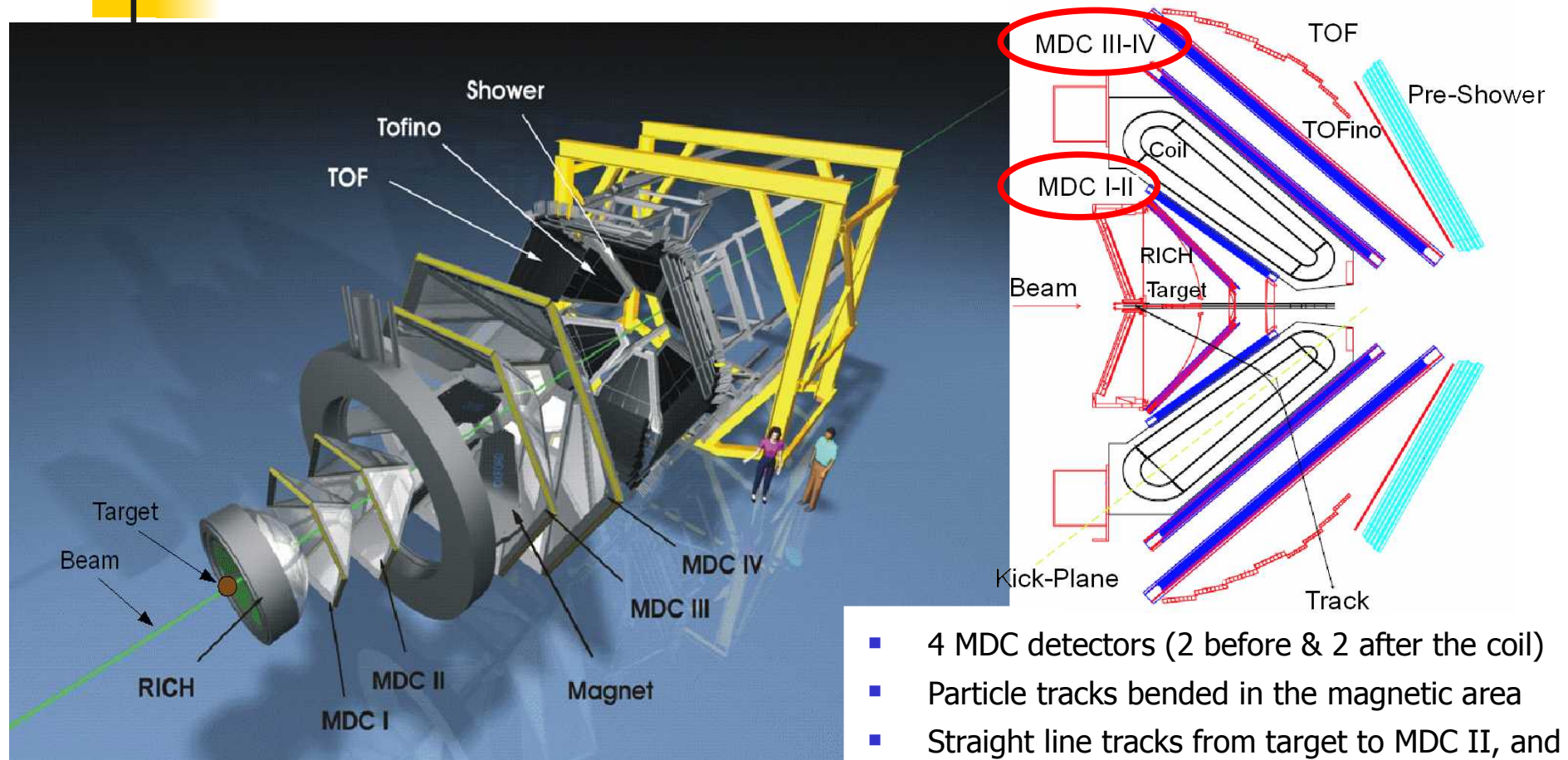
HADES detector system



- 4 MDC detectors (2 before & 2 after the coil)
- Particle tracks bended in the magnetic area
- Straight line tracks from target to MDC II, and from MDC III to MDC IV
- Currently focusing on the inner part, due to a similar principle



# Detector System for Particle Collisions

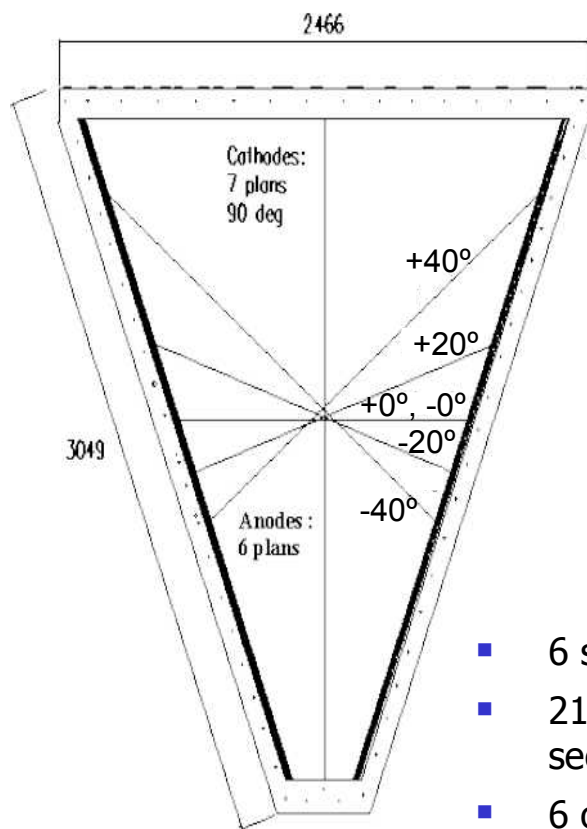


HADES detector system

- 4 MDC detectors (2 before & 2 after the coil)
- Particle tracks bended in the magnetic area
- Straight line tracks from target to MDC II, and from MDC III to MDC IV
- Currently focusing on the inner part, due to a similar principle

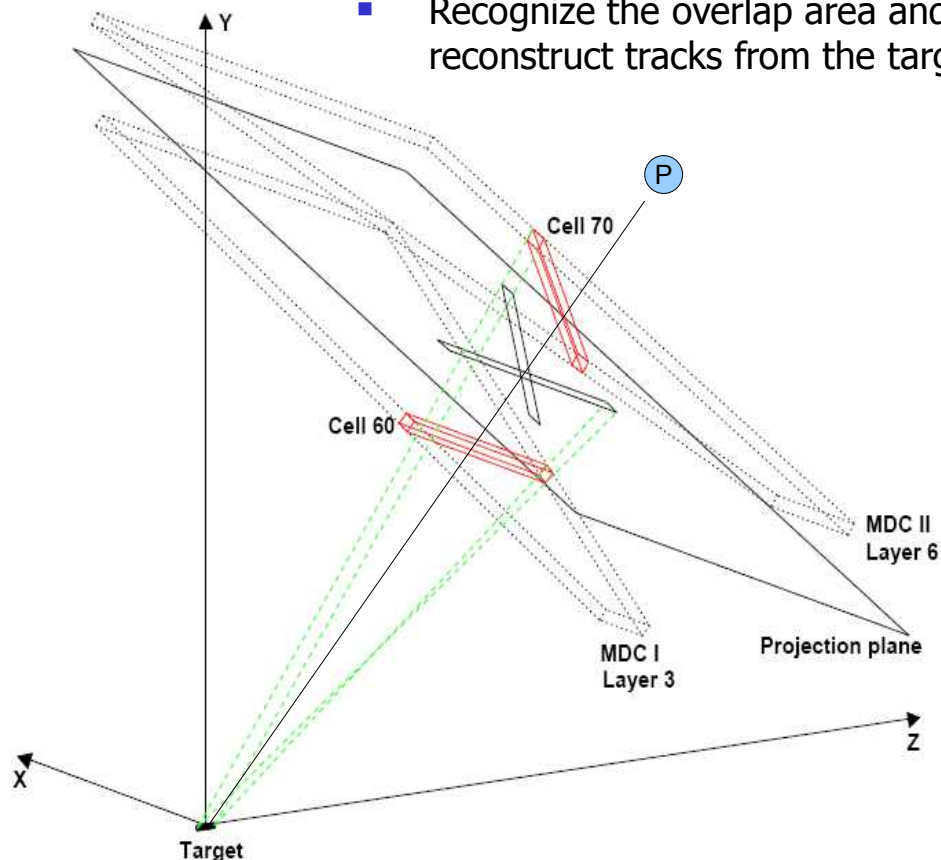
# Principle of the Tracking Algorithm

MDC – Chamber (front view)



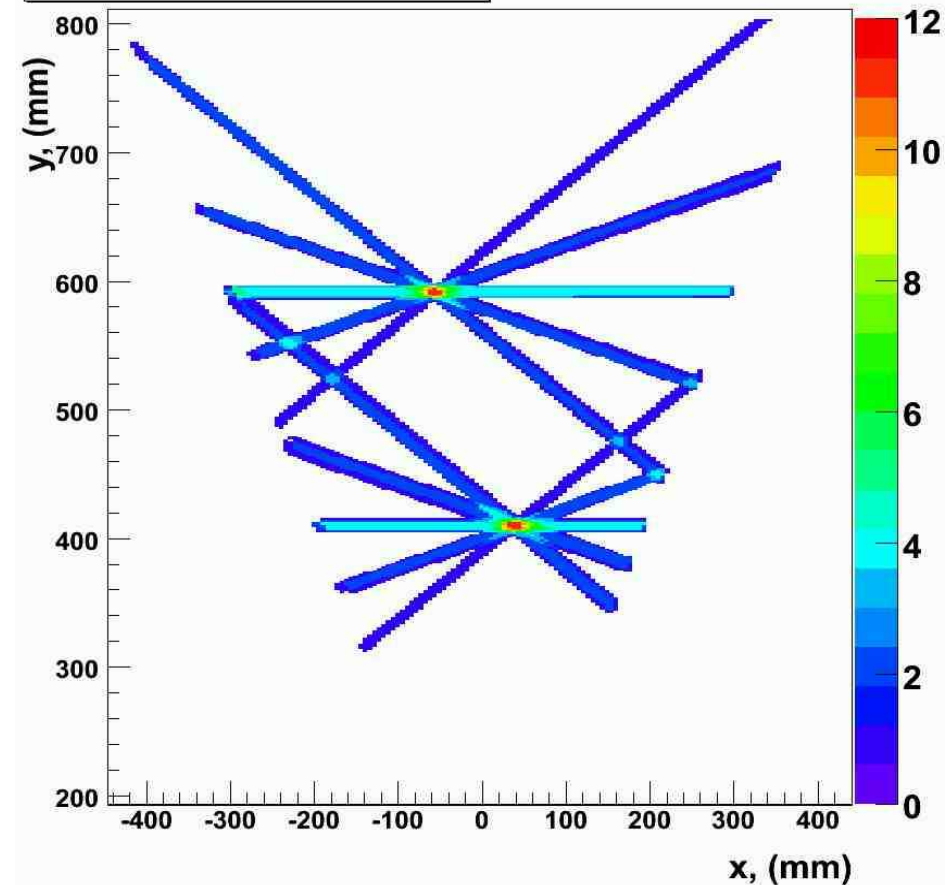
- 6 sectors
- 2110 wires per sector (inner)
- 6 orientations

- Wires fired by flying particles
- Project fired wires to a plane
- Recognize the overlap area and reconstruct tracks from the target

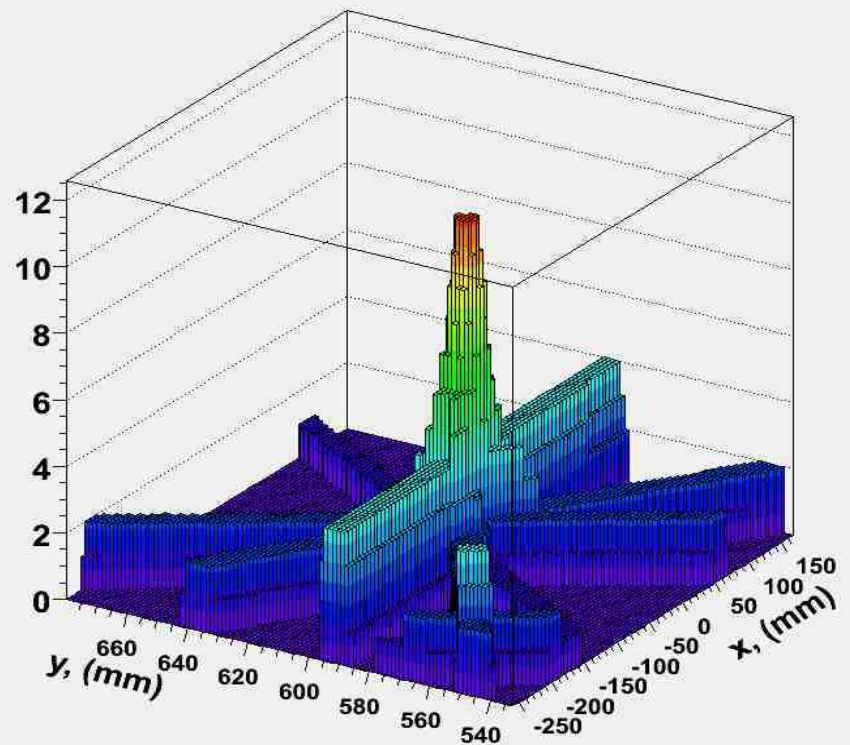


# Principle of the Tracking Algorithm

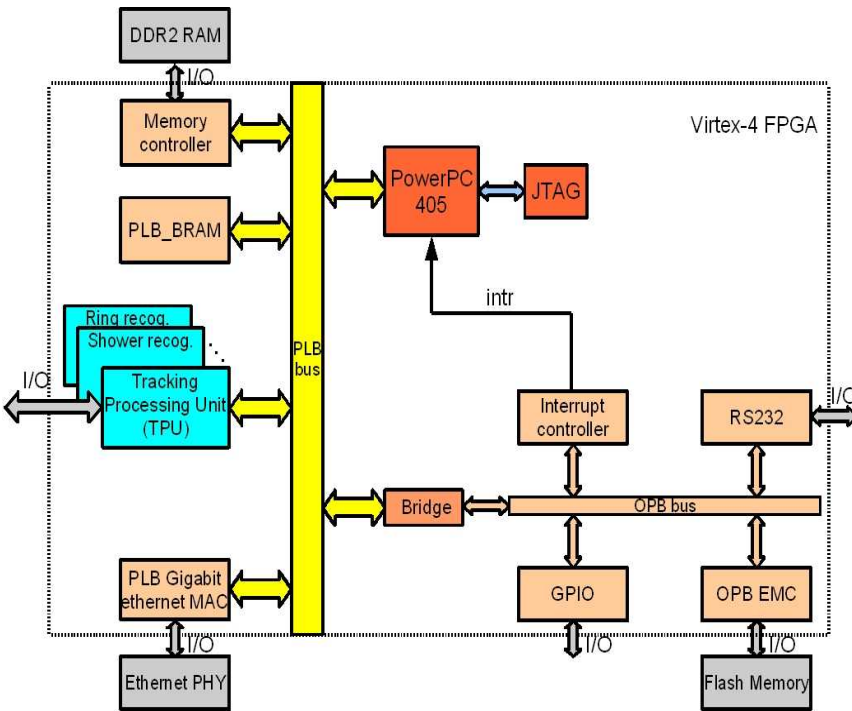
Event 74 Sector 4



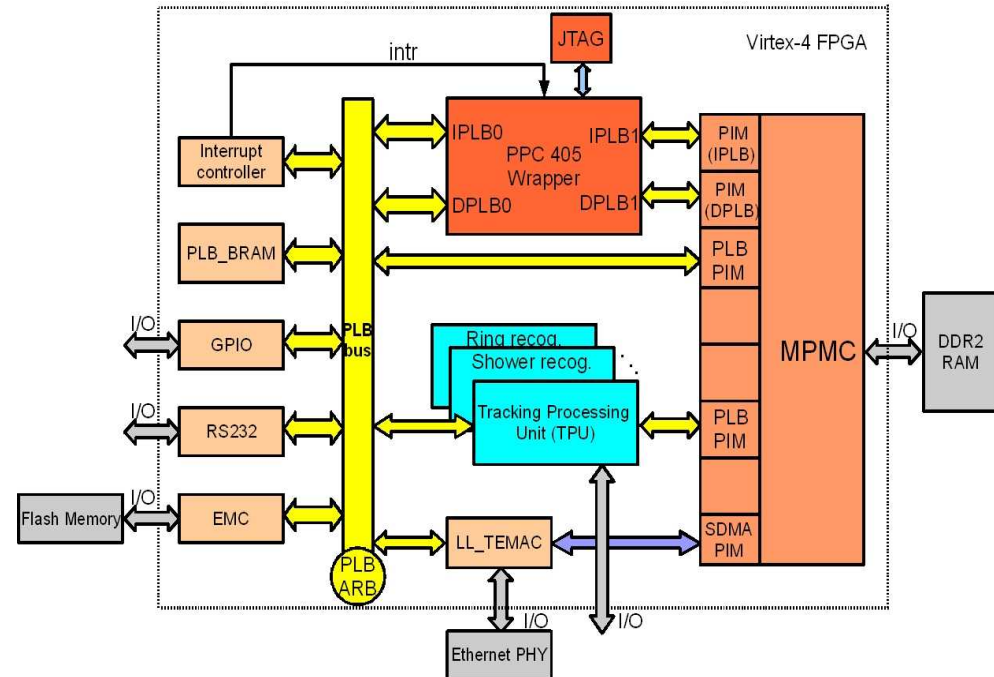
Event 74 Sector 4



# FPGA Node Development



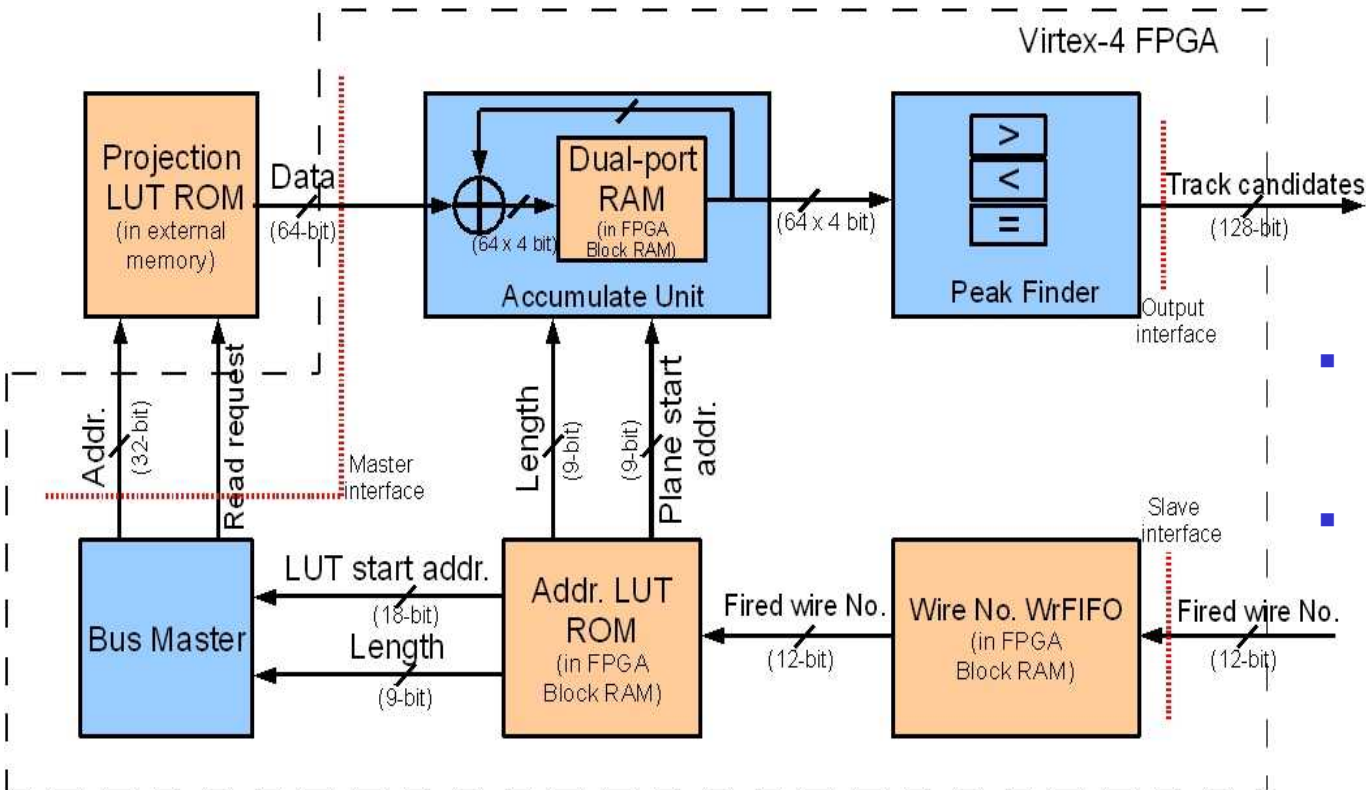
- Old bus-based architecture (PLB & OPB)
- CPU & Fast peripherals on PLB
- Slow peripherals on OPB
- Tracking Processing Unit (TPU) on PLB as a fast device



- New LocalLink-based architecture
- Multi-Port Memory Controller (8 ports)
- Direct access to the memory from the device
- TPU interfaced to MPMC directly

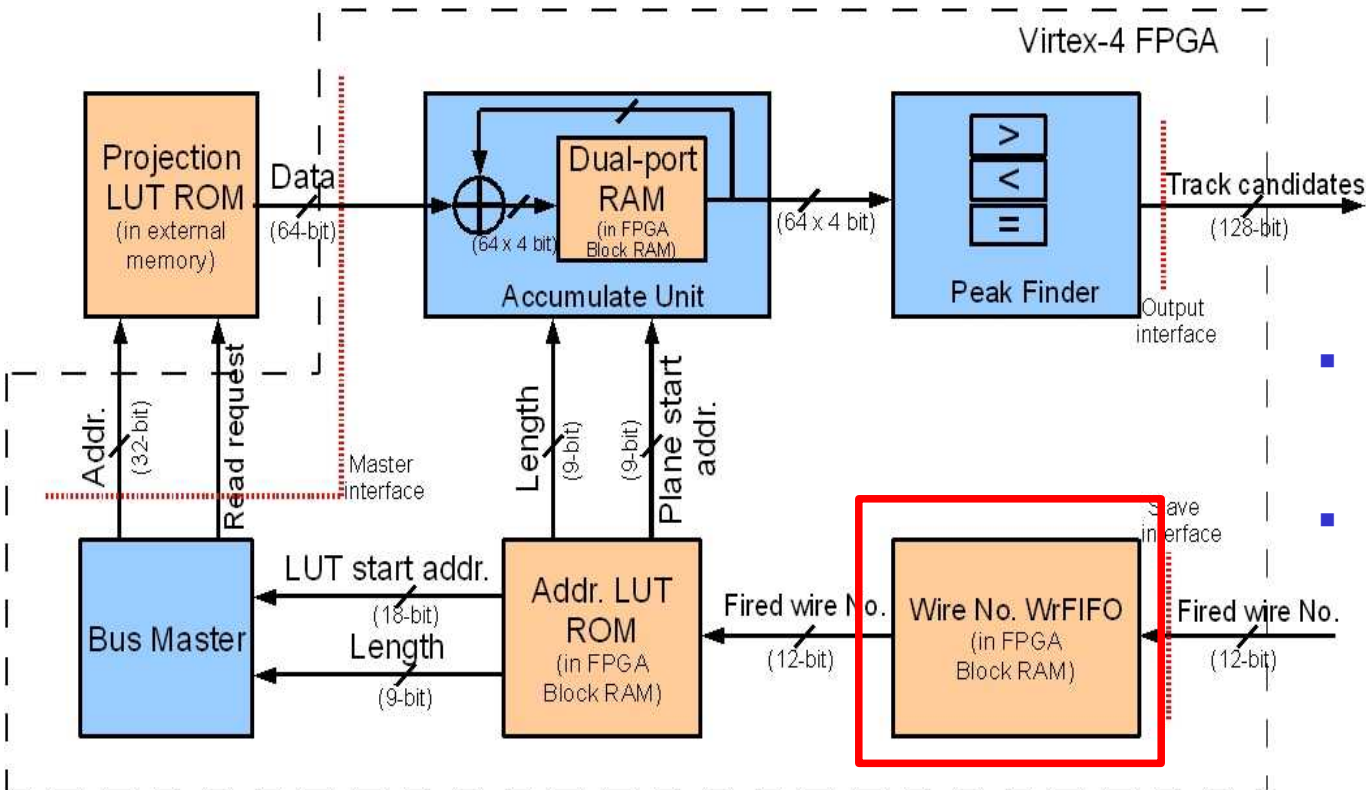


# TPU Design on FPGA



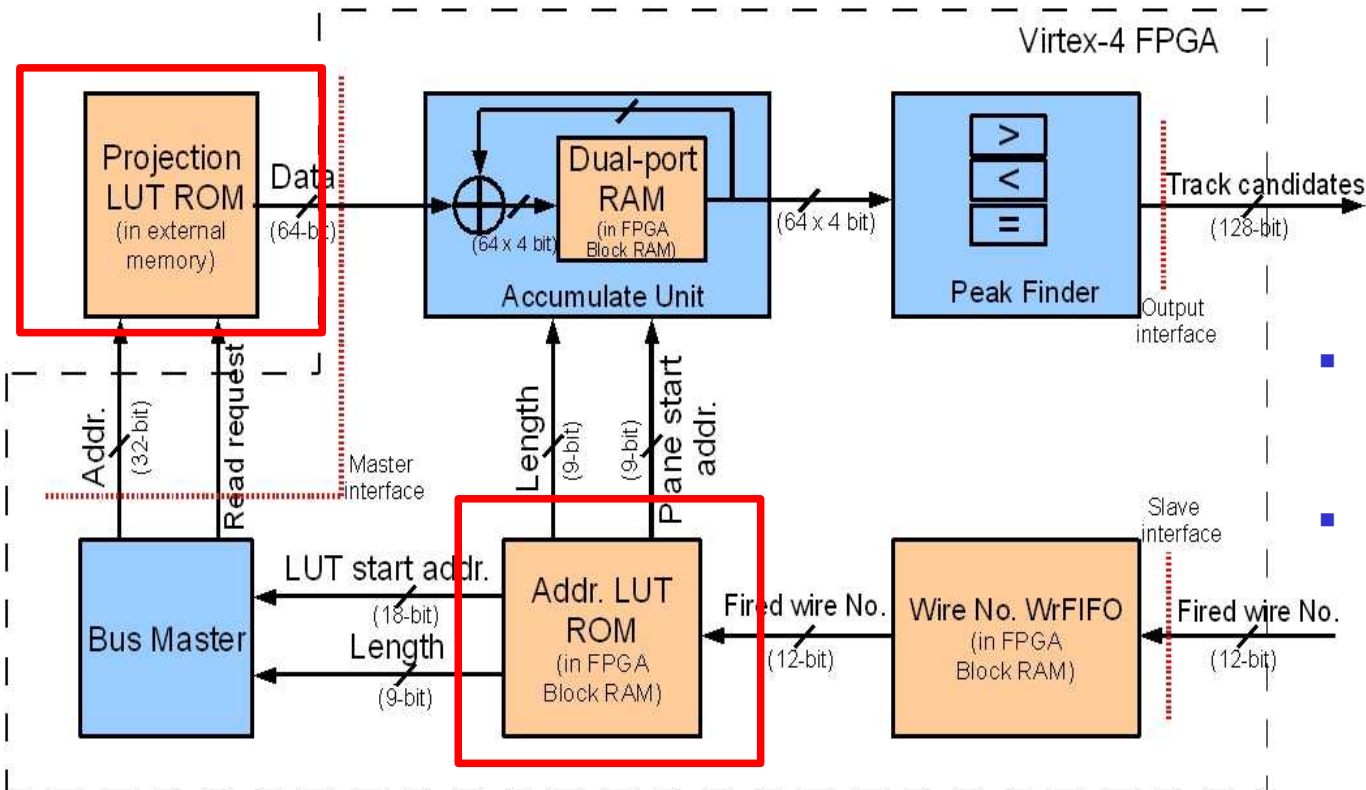
- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder

# TPU Design on FPGA



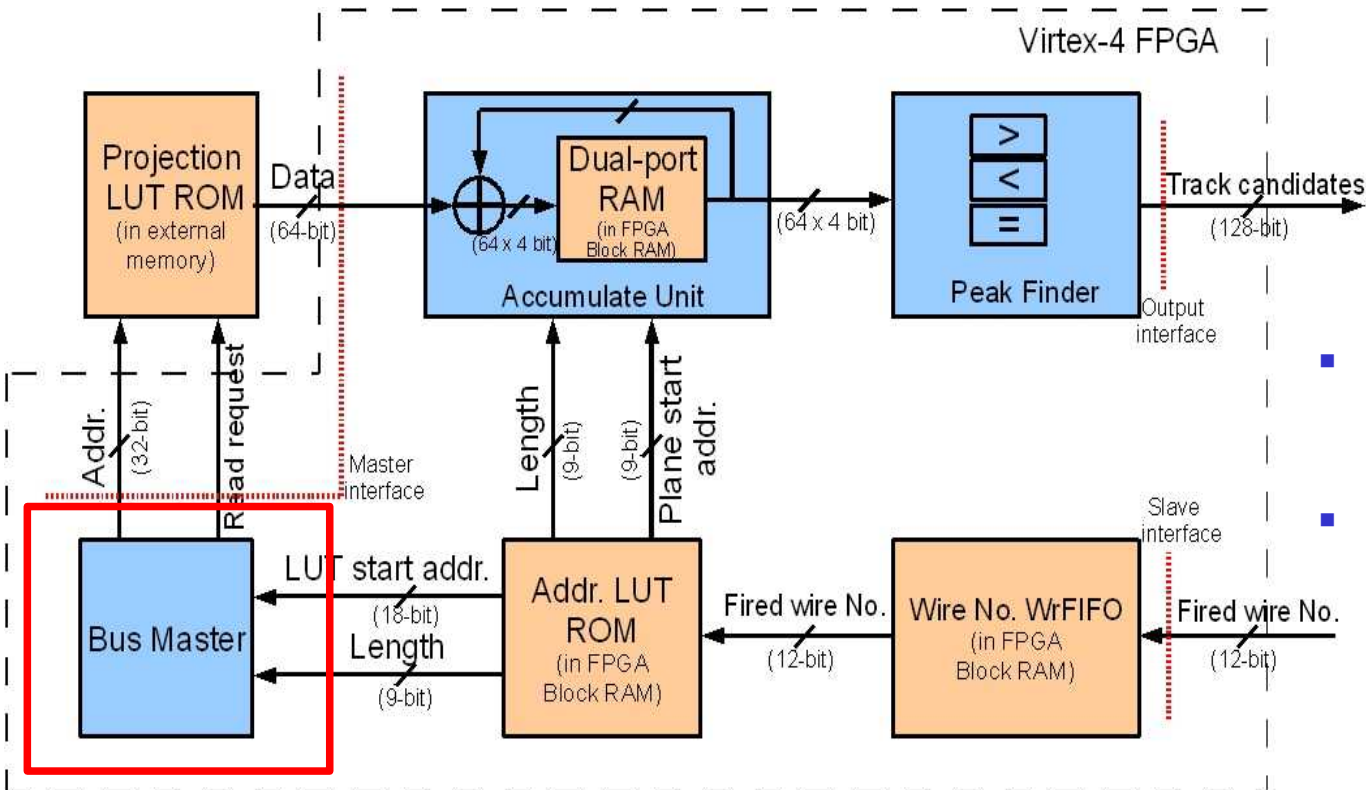
- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder

# TPU Design on FPGA



- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder

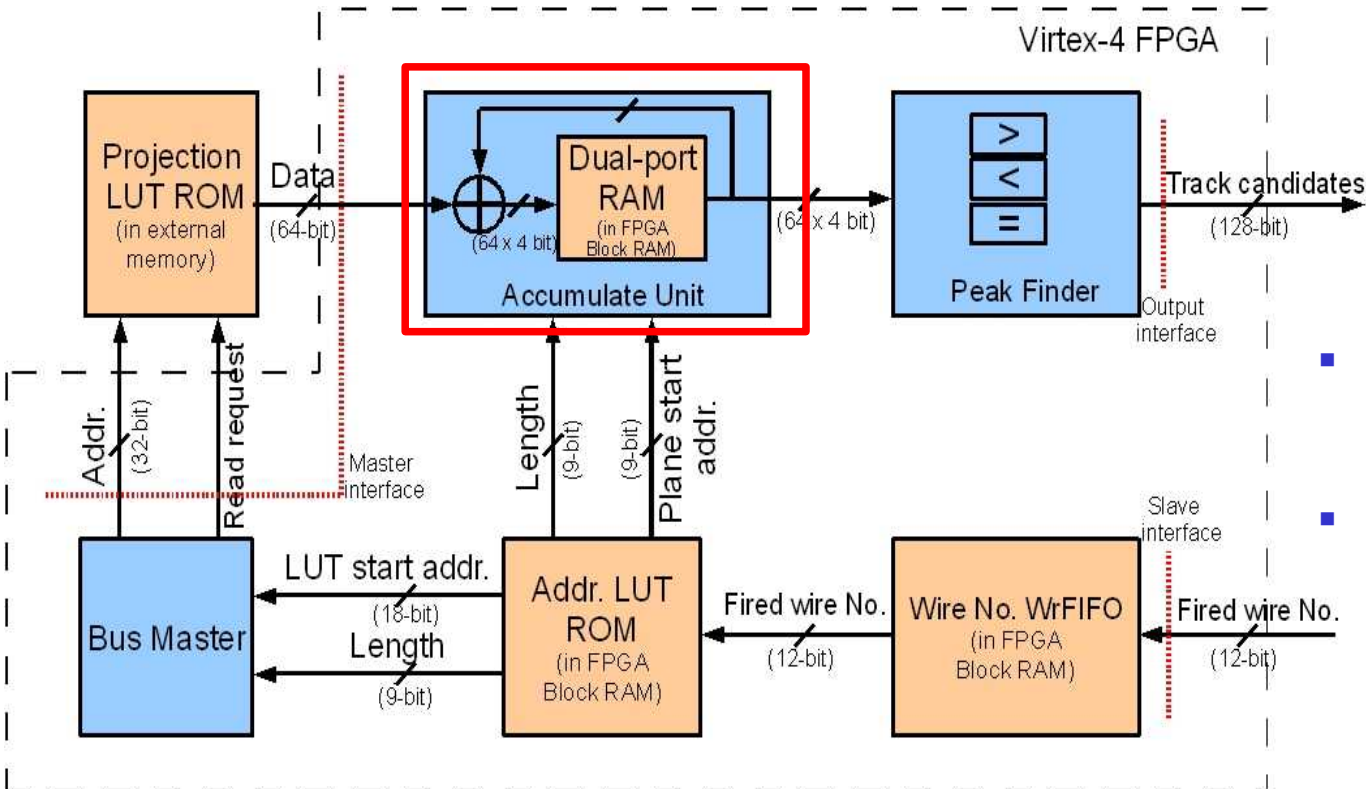
# TPU Design on FPGA



- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder

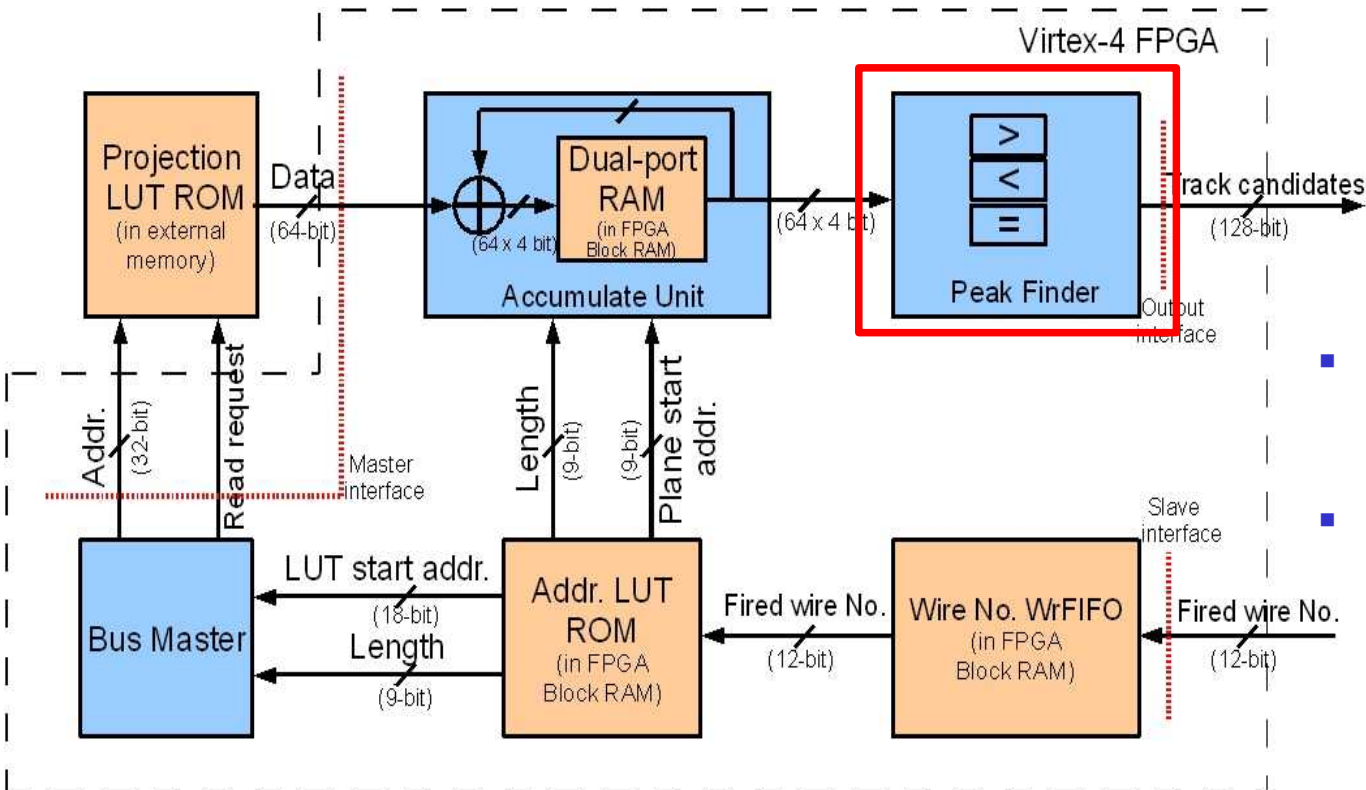


# TPU Design on FPGA



- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder

# TPU Design on FPGA



- Tracking Processing Unit (TPU) for track reconstruction computation
- Sub-modules:
  - Wire No. Write FIFO
  - Proj. LUT & Addr. LUT
  - Bus master
  - Accumulate unit
  - Peak finder



# Implementation Results

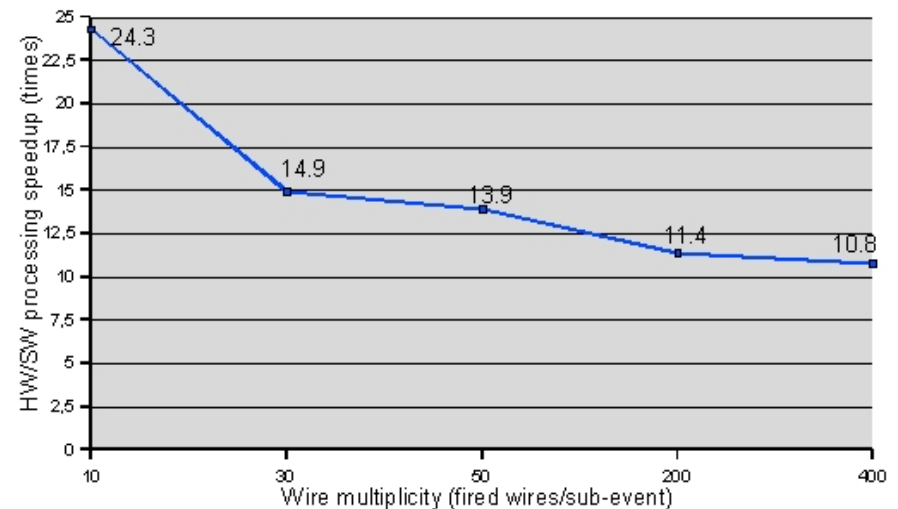
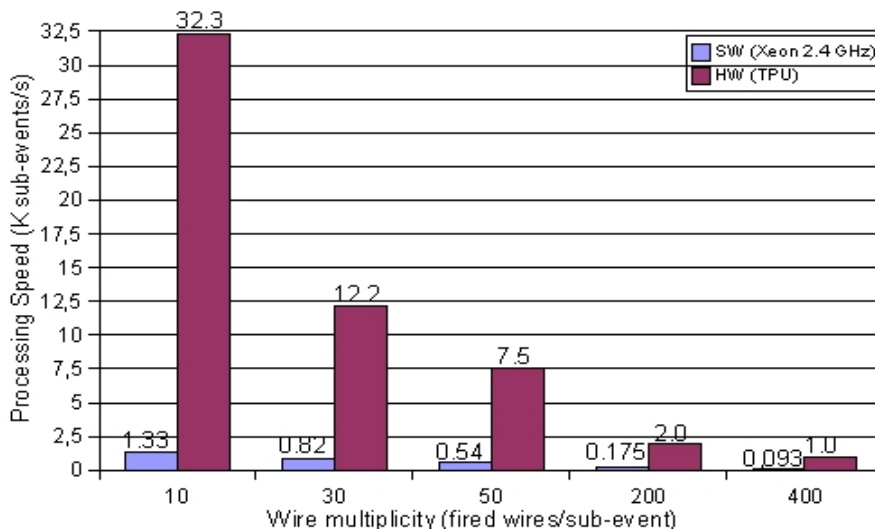
Resources	TPU	compute node platform	PLB-IPIF	system with TPU (sum)
<b>4-input LUTs</b>	5175 out of 50560 (10.2%)	8531 out of 50560 (16.9%)	2900 out of 50560 (5.7%)	16606 out of 50560 (32.8%)
<b>Slice Flip-Flops</b>	1715 out of 50560 (3.4%)	5724 out of 50560 (11.3%)	1640 out of 50560 (3.2%)	9079 out of 50560 (18.0%)
<b>Block RAMs</b>	41 out of 232 (17.7%)	18 out of 232 (7.8%)	0	59 out of 232 (25.4%)
<b>DSP Slices</b>	0	8 out of 128 (6.3%)	0	8 out of 128 (6.3%)

**Table 1. Resource consumption**

- Resource utilization of Virtex-4 FX60 FPGA -- acceptable!
- Timing limitation: 125 MHz without much optimization effort
- Clock frequency fixed at 100 MHz, to match the PLB speed

# Performance Evaluation

- MPMC-based structure used for measurements
- A C program running on the Xeon 2.4 GHz computer as the software reference
- Different measurement points on different wire multiplicities (10, 30, 50, 200, 400 fired wires out of 2110)
- Speedup of 10.8-24.3 times per module have been seen compared to the software solution.







## Conclusion and Future Work

---

- Basic principle of the inner track reconstruction for particle physics experiments was implemented on Xilinx FPGA.
- Integrated in the system design, the TPU module works to find out track candidates.
- Resource utilization is acceptable. The speedup of 10.8-24.3 times per module has been seen, compared to the software solution.
- Incorporate multiple modules in the system and make them work in parallel for high performance.
- Outer tracking implementation.



---

Thanks for your attention!