HW/SW Co-design of a General-Purpose Computation Platform in Particle Physics

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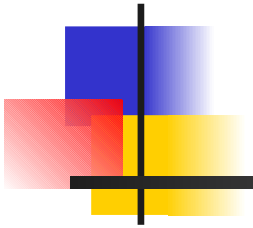
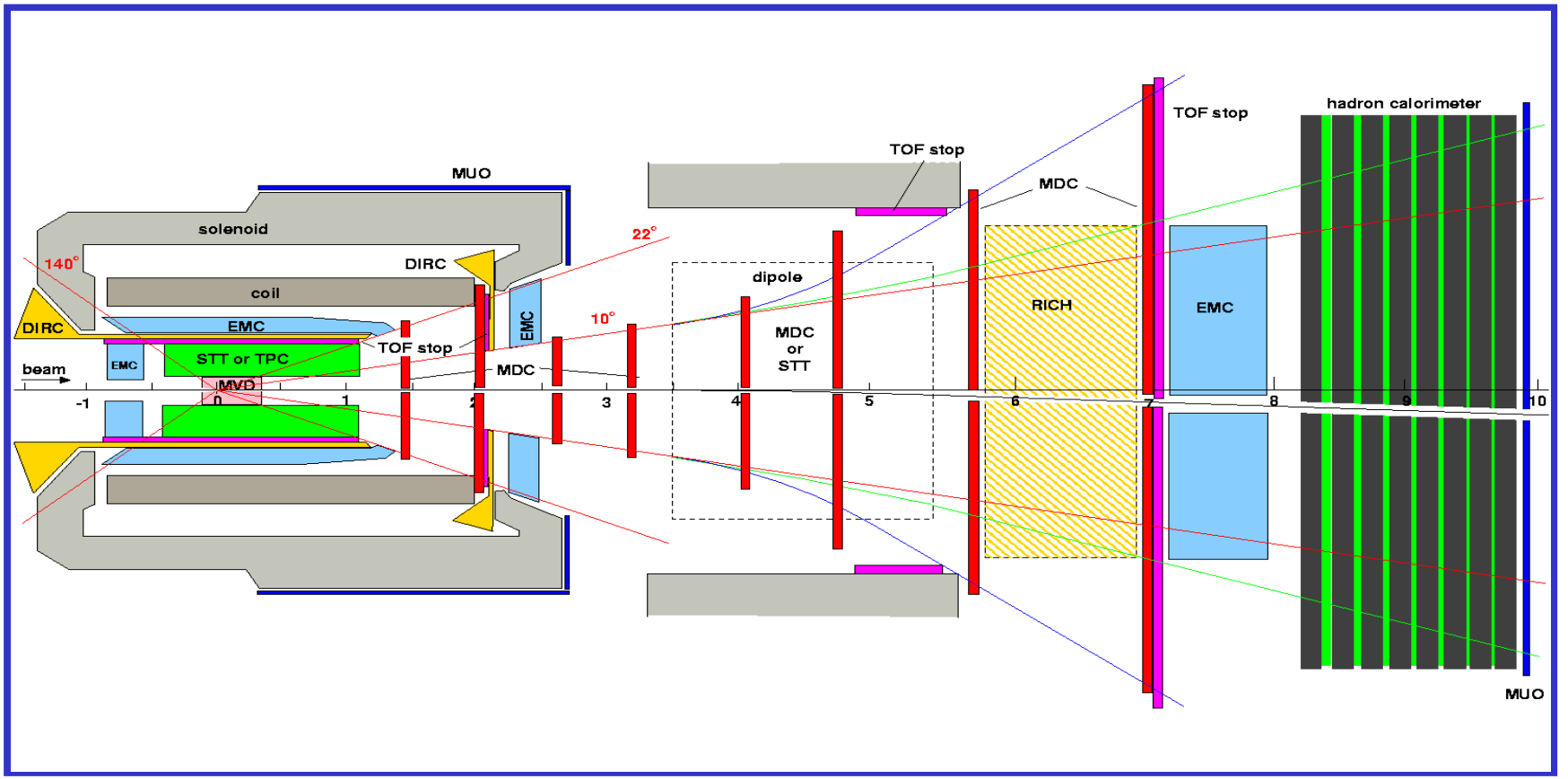


Outline

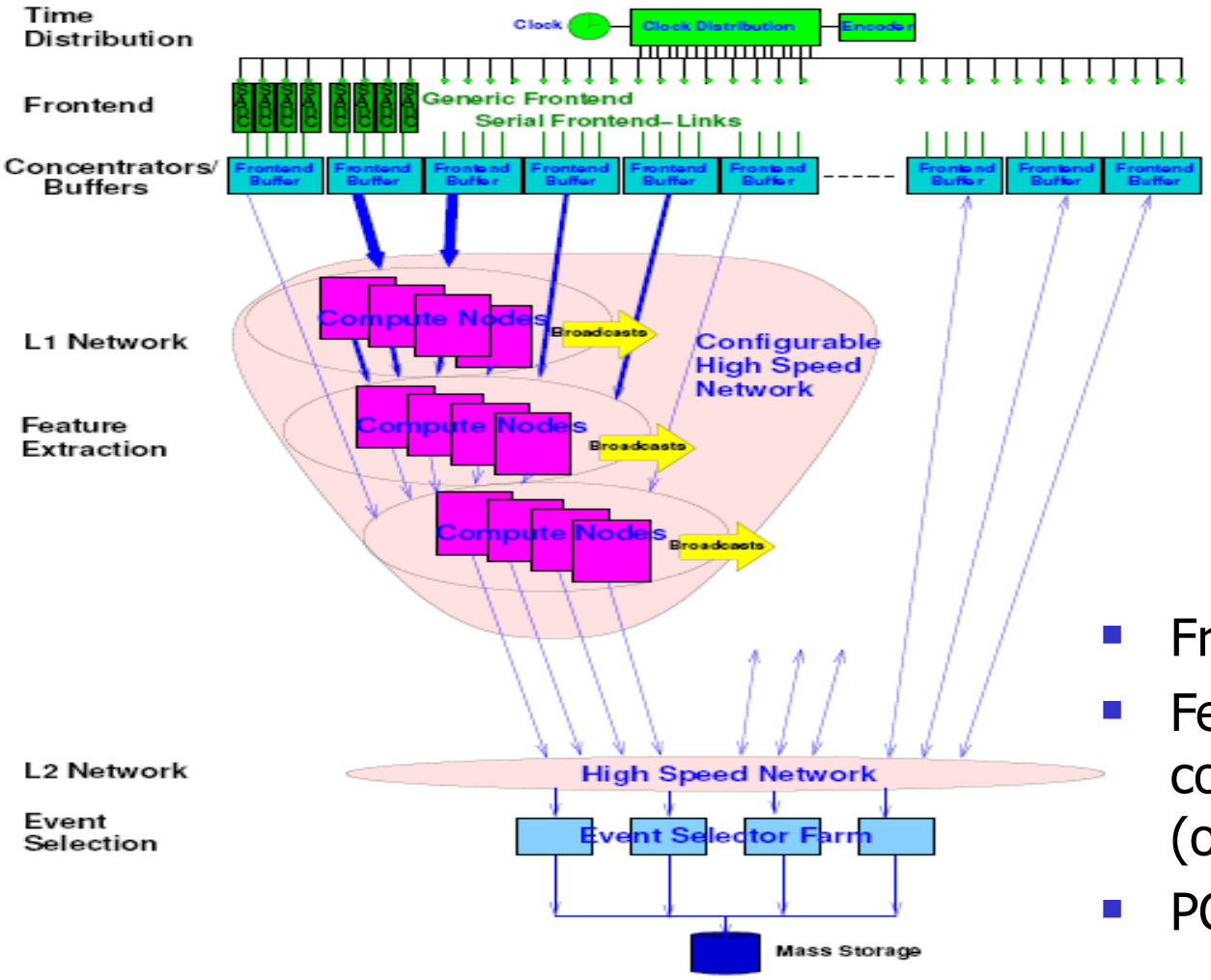
- Background & Motivation
- System Architecture
  - Network Architecture
  - Compute Node Architecture
- Partitioning Strategy
- HW Design
- SW Design
- Experimental Results
- Status and Outlook

Detector System in Physics Experiments

- Detectors: RICH, MDC, TOF ……
- Signals generated when particles fly through the detectors



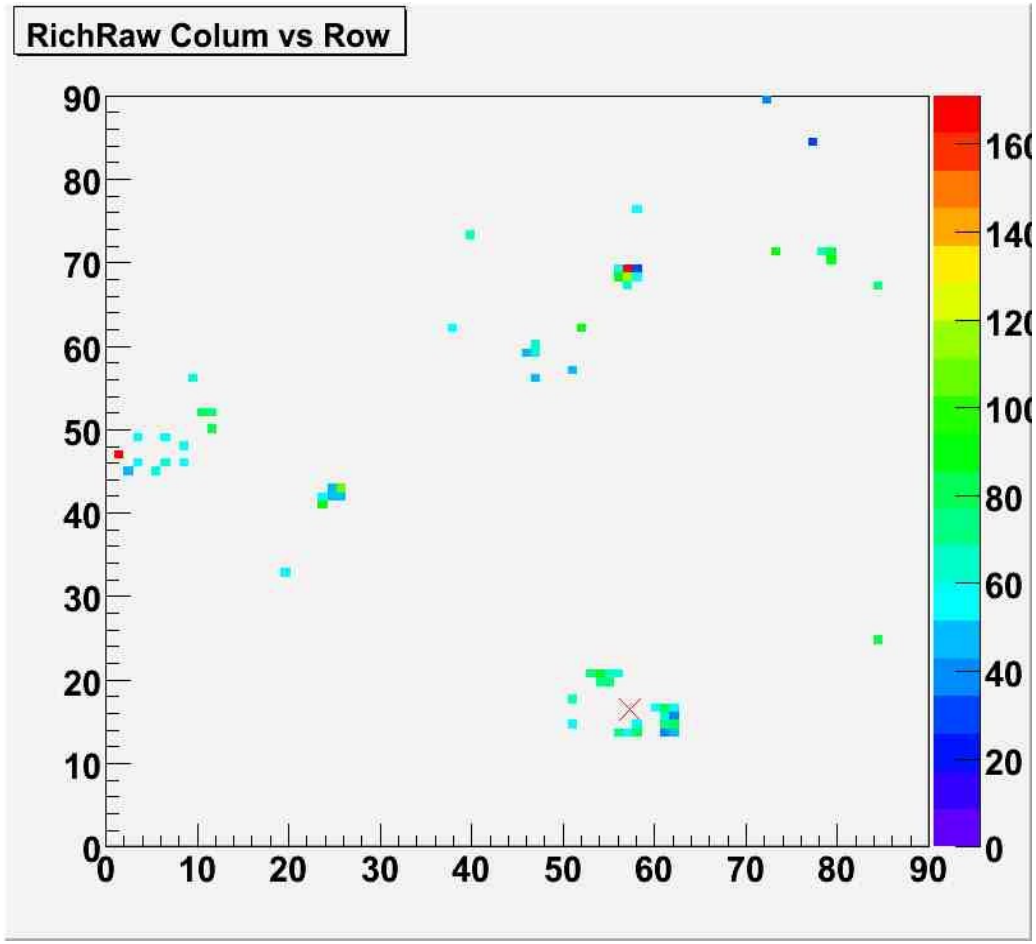
Data Acquisition System



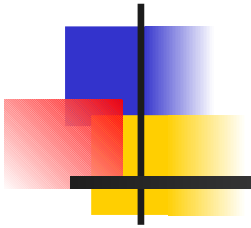
- Front-end electronics
- Feature extraction computation network (our focus)
- PC farm & mass storage

Feature Extraction Example

Ring recognition



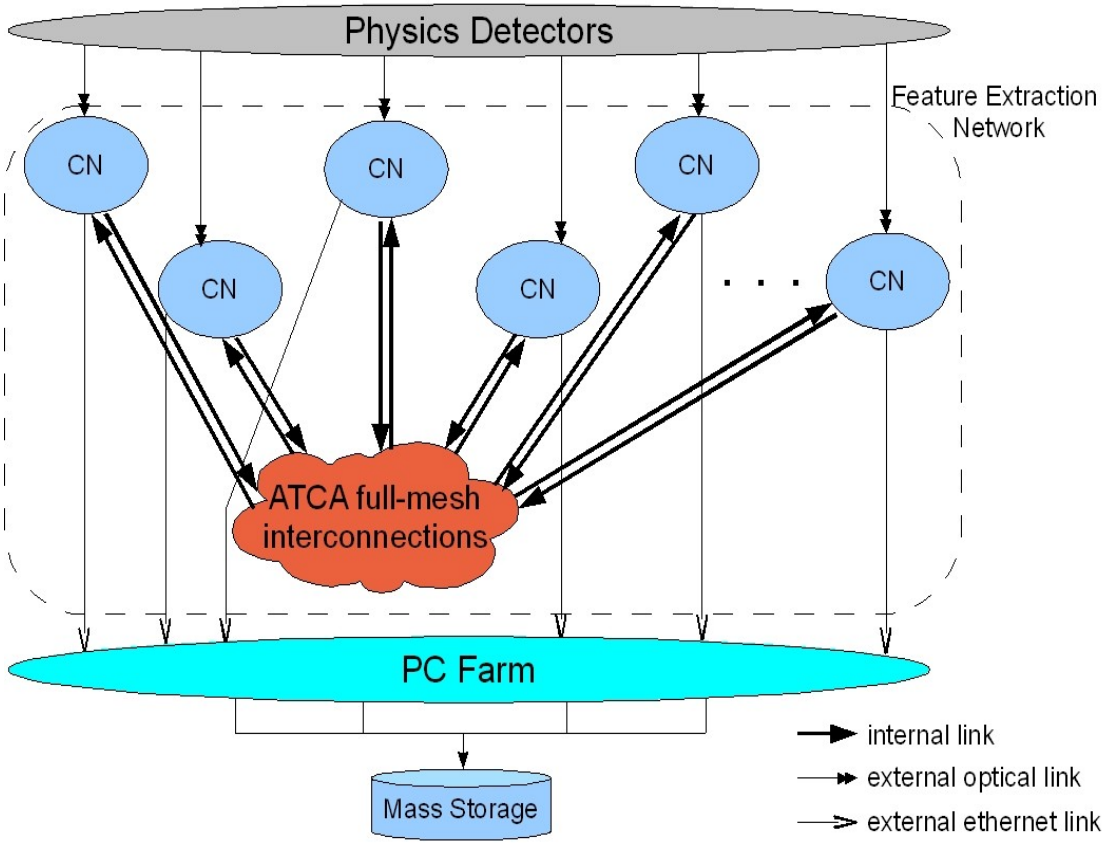
- Typically 36K pixels on the RICH detector in total
- Reaction rate @ 10 MHz
- Computation task: to scan all 36K pixels for rings per 100 ns
- Other even heavier computation tasks such as MDC track reconstruction, etc.
- HW parallel and pipelined processing in FPGA to achieve the high performance.



Motivation

- The DAQ system in modern nuclear and particle physics experiments desires:
  - High data processing capability. (reaction rate up to 20MHz, data rate up to 200 GB/s)
  - Various on-line feature extraction algorithms. (Ring recog., MDC tracking, etc.)
  - To be general-purpose for different experiments.
  - To be highly and remotely reconfigurable.
- Purpose:
  - To design the system, based on the platform FPGA technology and HW/SW co-design.

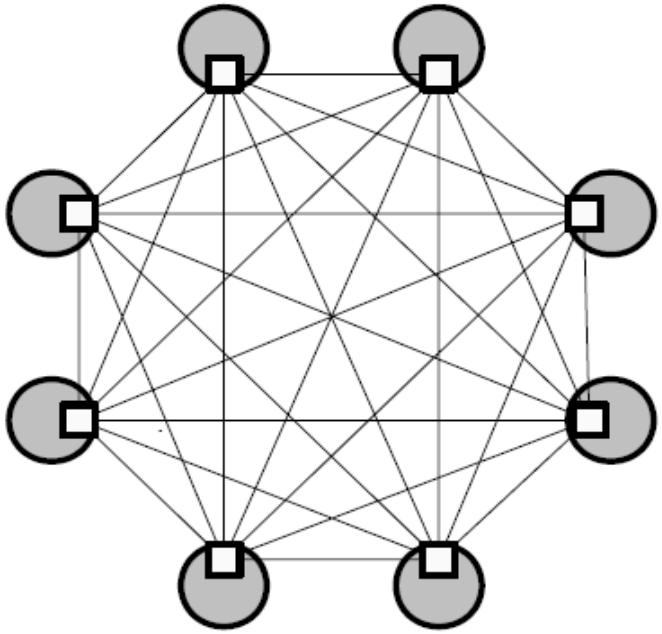
Network Architecture



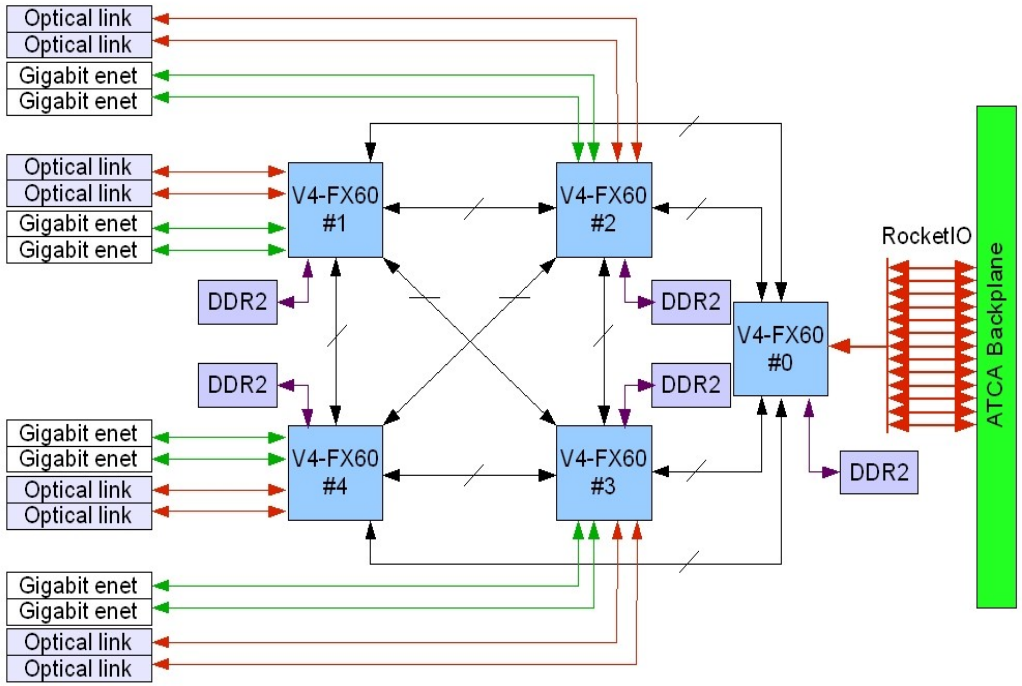
- Feature extraction algo. implemented in the computation network.
- Compute node boards internally interconnected by the full-mesh ATCA backplane.
- External interconnections:
  - Optical links
  - Gigabit Ethernet

ATCA Full-mesh Backplane

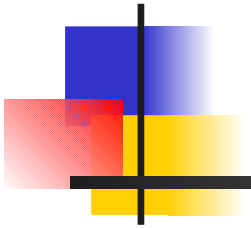
- Full-mesh backplane network
- High flexibility to correlate results from different algorithms
- High performance



Compute Node (CN) Architecture



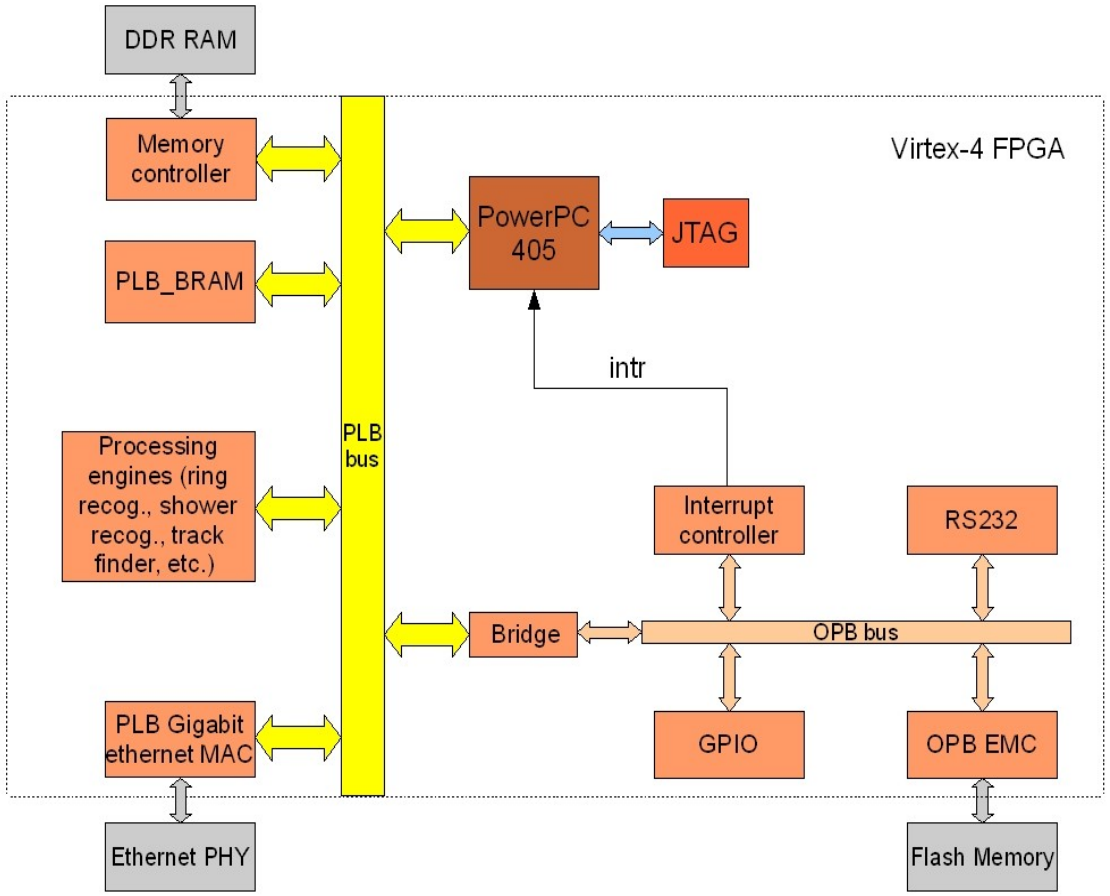
- Prototype board with 5 Xilinx Virtex-4 FX60 FPGAs
- 4 FPGAs as algo. processors
- 1 FPGA as a switch
- Full-mesh communication on-board
- External links:
  - Optical links
  - Gigabit Ethernet



Partitioning Strategy

- Computation-intensive algorithms implemented in the FPGA fabric for high performance.
- Parallel and pipelined computation in HW.
- Slow controls in SW (OS + Applications):
  - To remotely upgrade the HW and SW designs.
  - Network test and measurement.
  - To display and modify the experimental parameters.
  - ……
- Soft TCP/IP stack in Linux OS.

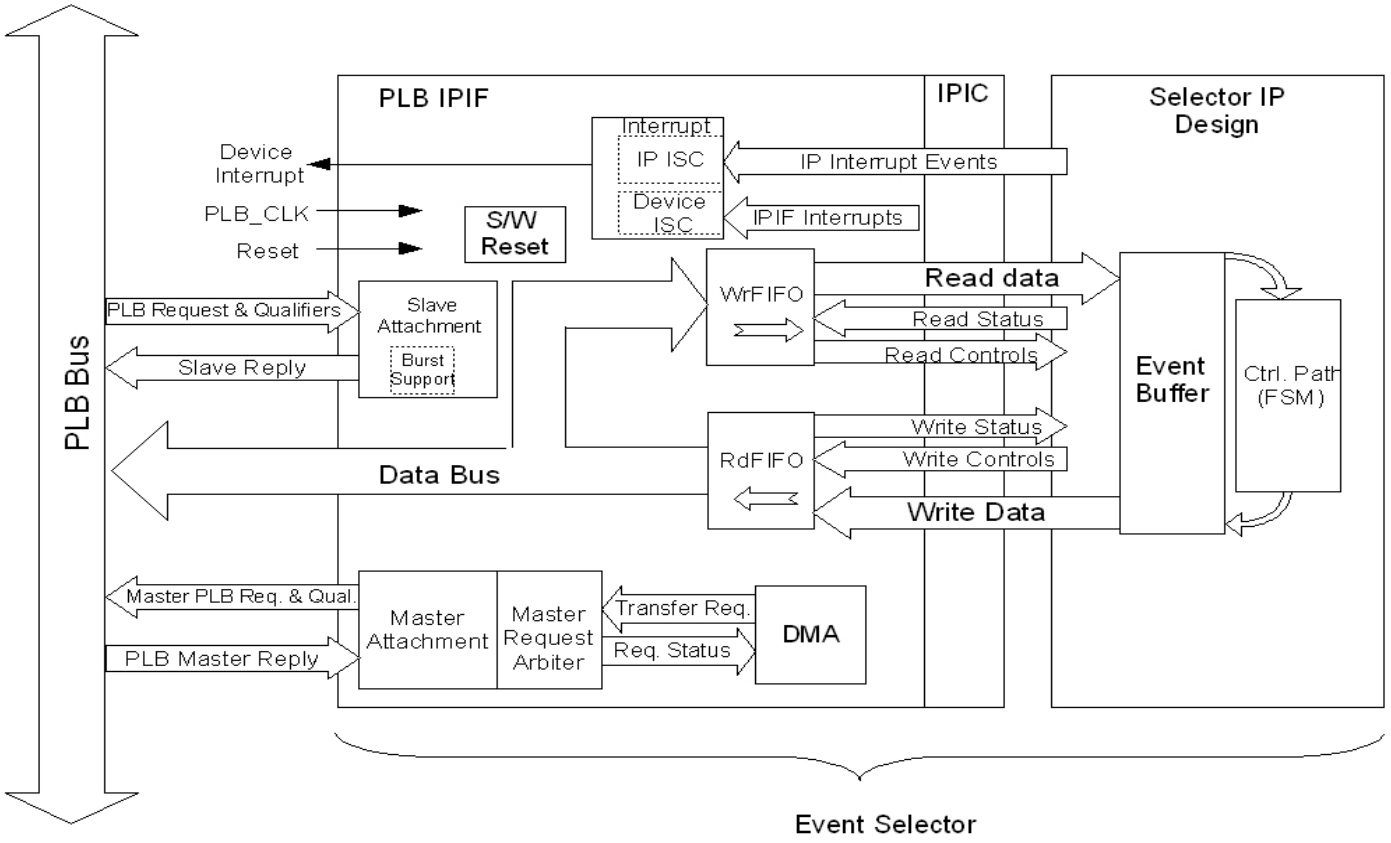
HW Design (FPGA Node)



- Bus-based platform
  - PLB (fast)
  - OPB (slow)
- PowerPC 405 CPU
- Algo. Processing engines
- Other peripherals:
  - Gigabit Ethernet
  - DDR memory
  - Flash memory
  - RS232
  - ……

HW Design (toy-model event selector)

- Event selector as a simple instance of the algo. processing engines:



SW Design

- Open-source embedded Linux on the embedded PowerPC
- Device drivers:
  - For Ethernet, RS232, Flash memory, etc.
  - For the customized processing modules
- Applications for slow controls:
  - High level scripts
  - C/C++ programs

Implementation Results

- Experiment platform: Xilinx Dev. Board ML403
- Virtex-4 FX 12 platform FPGA
- In the real product: Virtex-4 FX 60
- Softwares:
  - XPS 8.2
  - ISE 8.2
  - Modelsim 6.1e
  - Bus Functional Models (BFM)
- PLB bus: 100 MHz
- PowerPC: 300 MHz

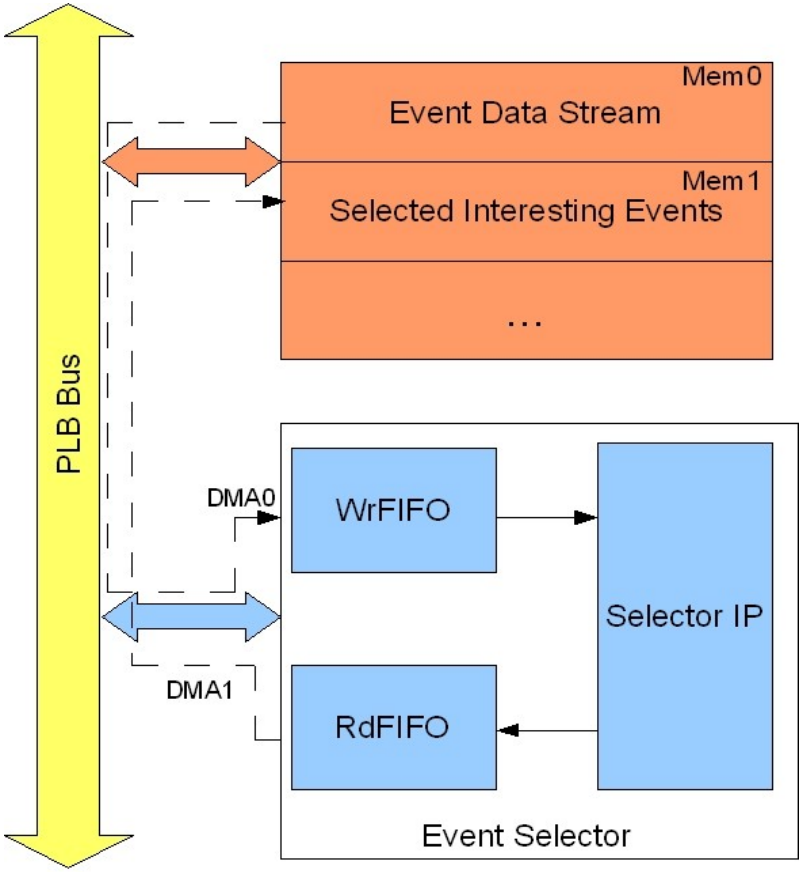
Resources	System without computing engine	Tri-mode Ethernet	*Event Selector* module (4kBytes WrFIFO RdFIFO and Event Buffer)
4-input LUTs	8531 out of 10944 (77%)	5346 out of 10944 (48%)	4674 out of 10944 (43%)
Slice Flip-Flops	5724 out of 10944 (52%)	4093 out of 10944 (37%)	2830 out of 10944 (25%)
FIFO16/ RAMB16s	18 out of 36 (50%)	18 out of 36 (50%)	6 out of 36 (17%)
DSP48s	8 out of 32 (25%)	8 out of 32 (25%)	0
DCMs	3 out of 4 (75%)	0	0

Communication Speed per Ethernet link

Protocol Type	Direction	Max. Throughput (Mbps)
UDP/IP	Board → PC	394.5 (TX)
UDP/IP	PC → Board	$\geq 394.5^{1}$ (RX)
TCP/IP	Board → PC	297.8
TCP/IP	PC → Board	316.6

- Board to PC, p2p interconnection of Gigabit Ethernet
- All features enabled to improve the communication speed, such as jumbo frame, S/G DMA, check-sum offloading, etc.
- Embedded PowerPC 405 CPU is the bottleneck: only 300 Mhz
- Results matching the thumb rule: 1 bps ~ 1 hz

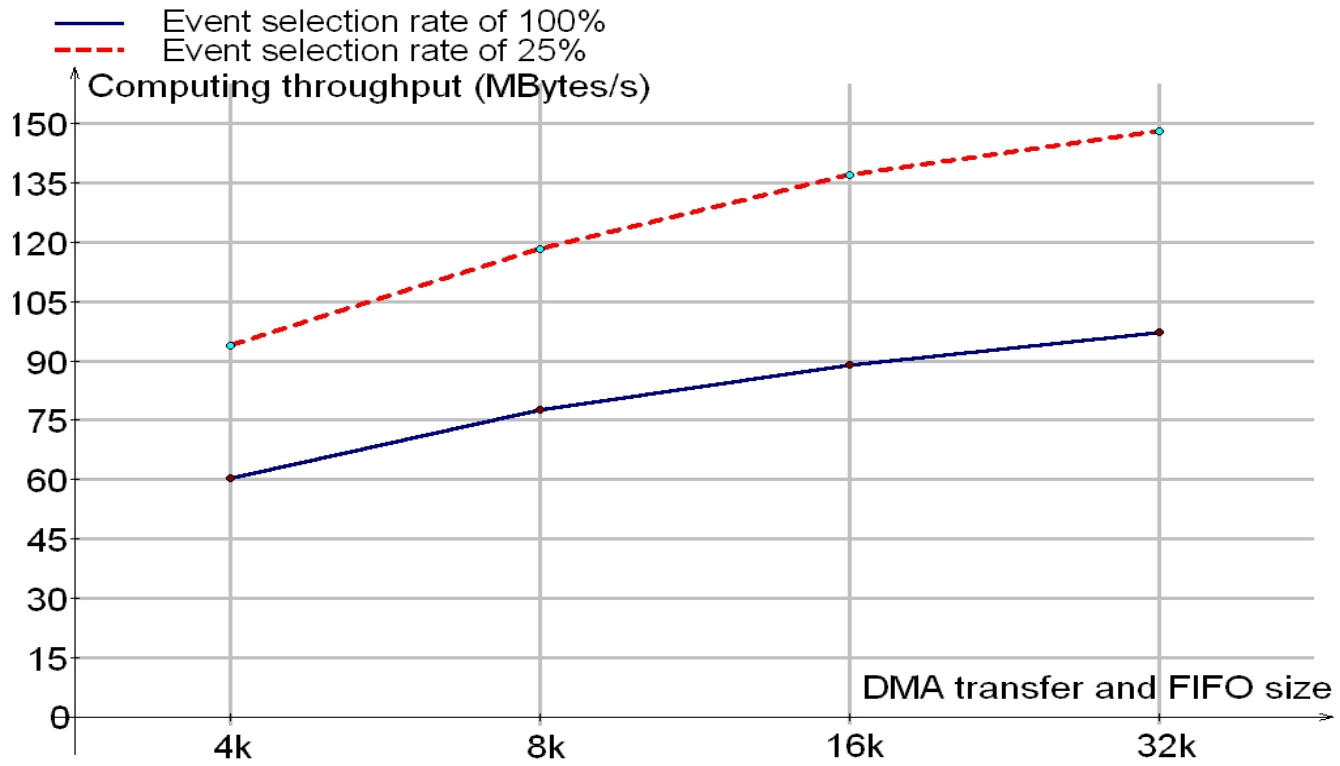
Computing Throughput of Event Selector



- Performance measurements of the event selector
- Experimental setup
  - Two DDR blocks
  - Event selector connected to the PLB
  - DMA transfers to feed data and collect results
  - 100% and 25% interesting event rates
- Calculation:

$$\text{Computing throughput} = \frac{\text{Data size}}{\text{Time}}$$

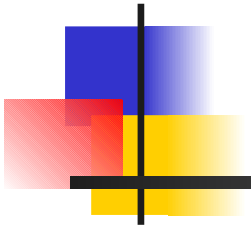
Computing Throughput of Event Selector



- Maximum results (32 KB FIFOs):
  - 148.1 MB/s (25% interesting event rate)
  - 97.3 MB/s (100% interesting event rate)

Status and Outlook

- Algorithm designs in FPGA fabric
  - Ring recognition for RICH detector
  - Particle track reconstruction (tracking) for MDC detectors
  - TOF processing for TOF detector
  - Shower recognition for Shower detector
  - Event builder
- Algorithm partition and distribution in CNs for parallel processing
- PCB layout for the CN boards
  - Prototype board ready in the early next year
- System implementation & debugging



Summary

- Motivation
  - Computation network with high processing capabilities in physics experiments
  - Reconfigurable general-purpose platform
  - Feature extraction algorithms
- Solution:
  - Co-design and FPGA based computation platform
- Results:
  - Implementation results
  - Communication and computation performance measurements
- Future work
  - Feature extraction algorithm implementations
  - Network study for parallel processing

Thanks for your attention!