JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Compute Node Design and Algorithm Development for the HADES DAQ and Trigger System

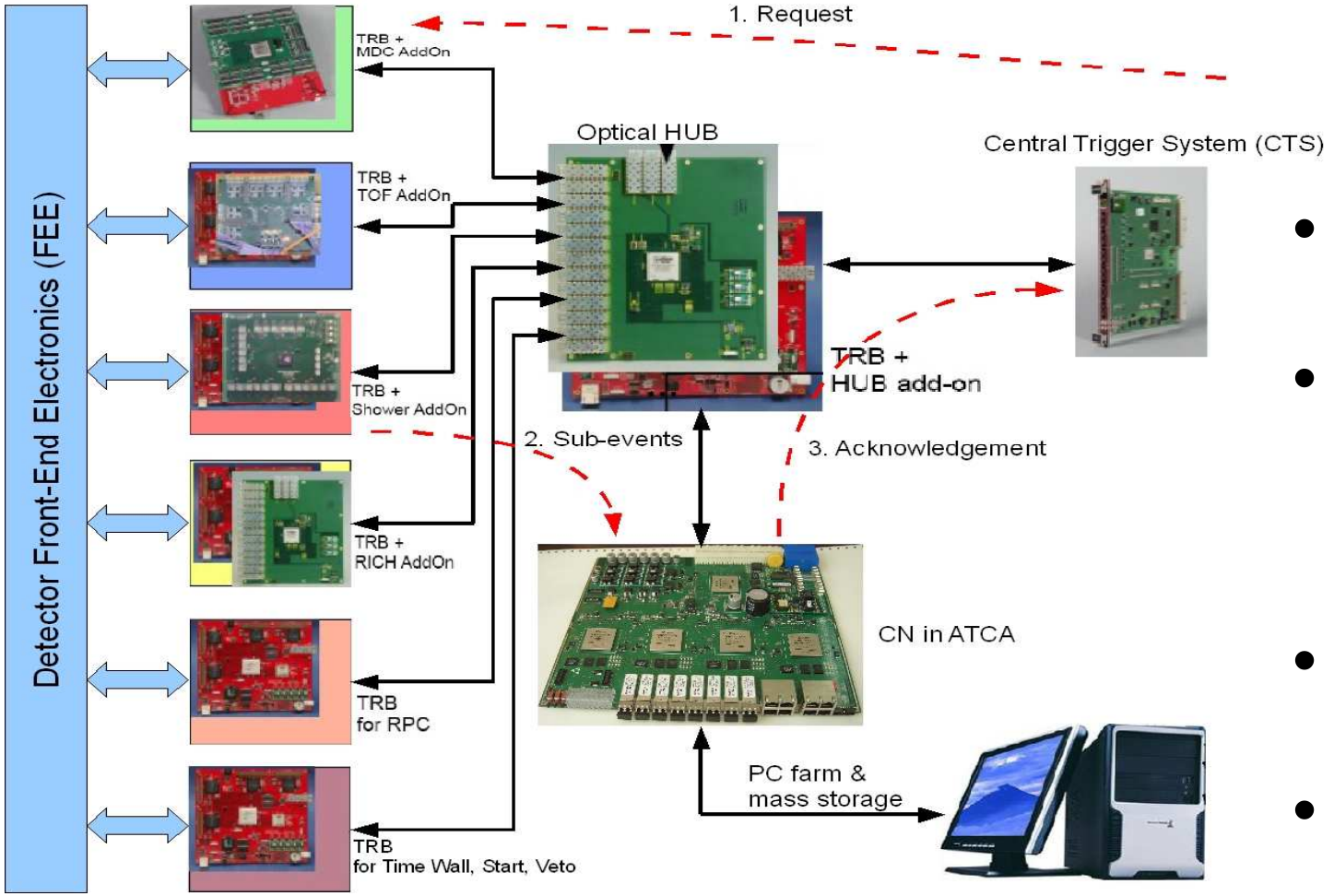
Justus-Liebig University Giessen

Presented by Ming Liu
for the HADES DAQ&T Collaboration Group

Outline

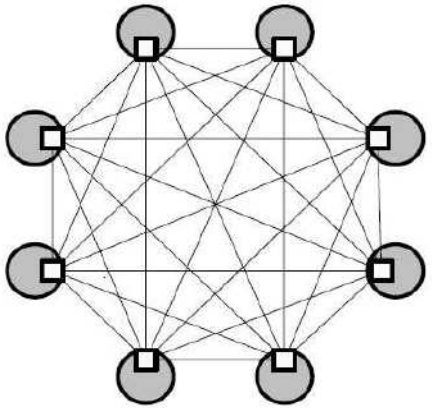
- HADES DAQ & trigger system
- Compute Node (CN) design
- Algorithm development on FPGAs
- Current status and outlook

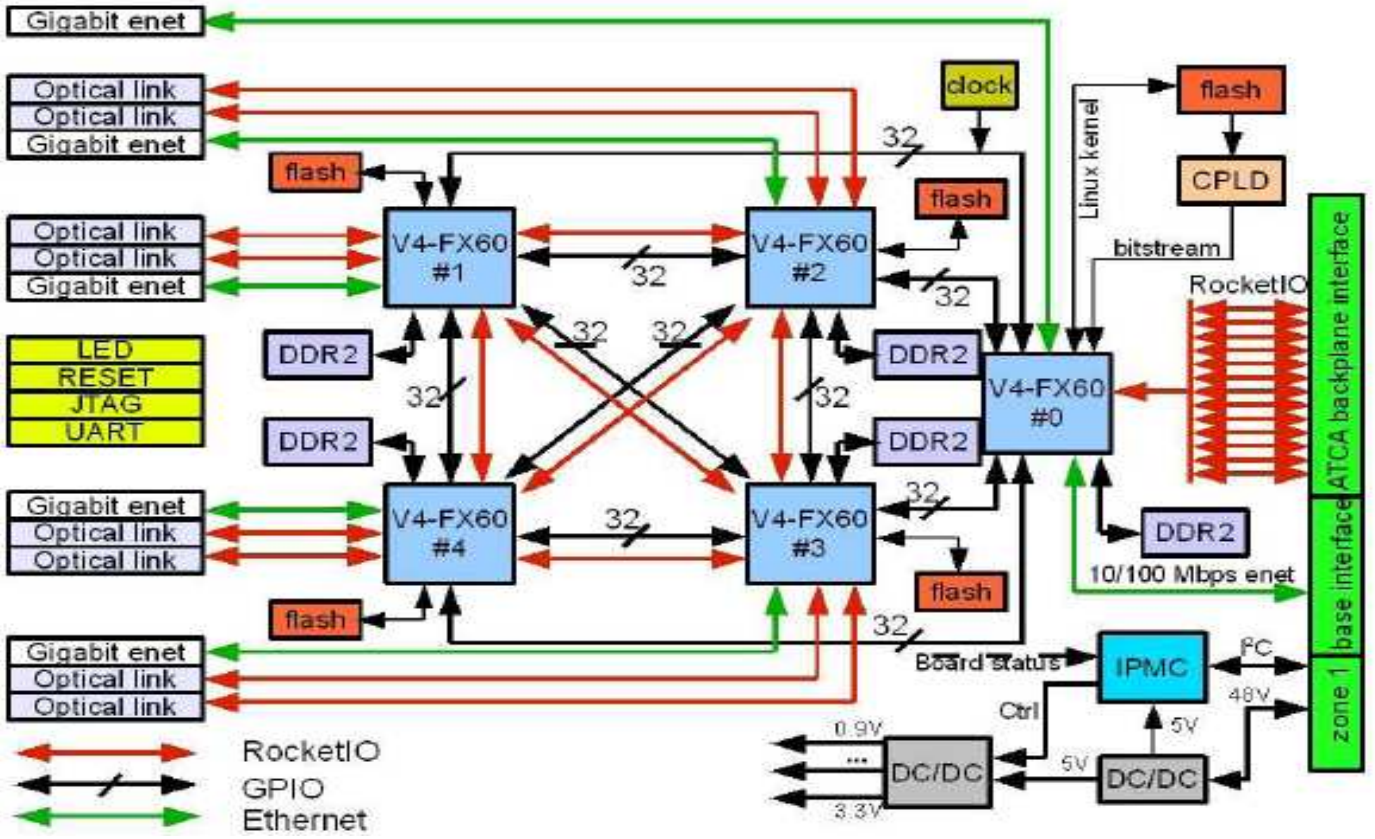
HADES DAQ and Trigger System



- TRBnet (Jan Michel, DPG'09)
- ATCA-based CNs for pattern recognition algorithms
- Central Trigger System (CTS)
- Mass storage

Compute Node HW Design

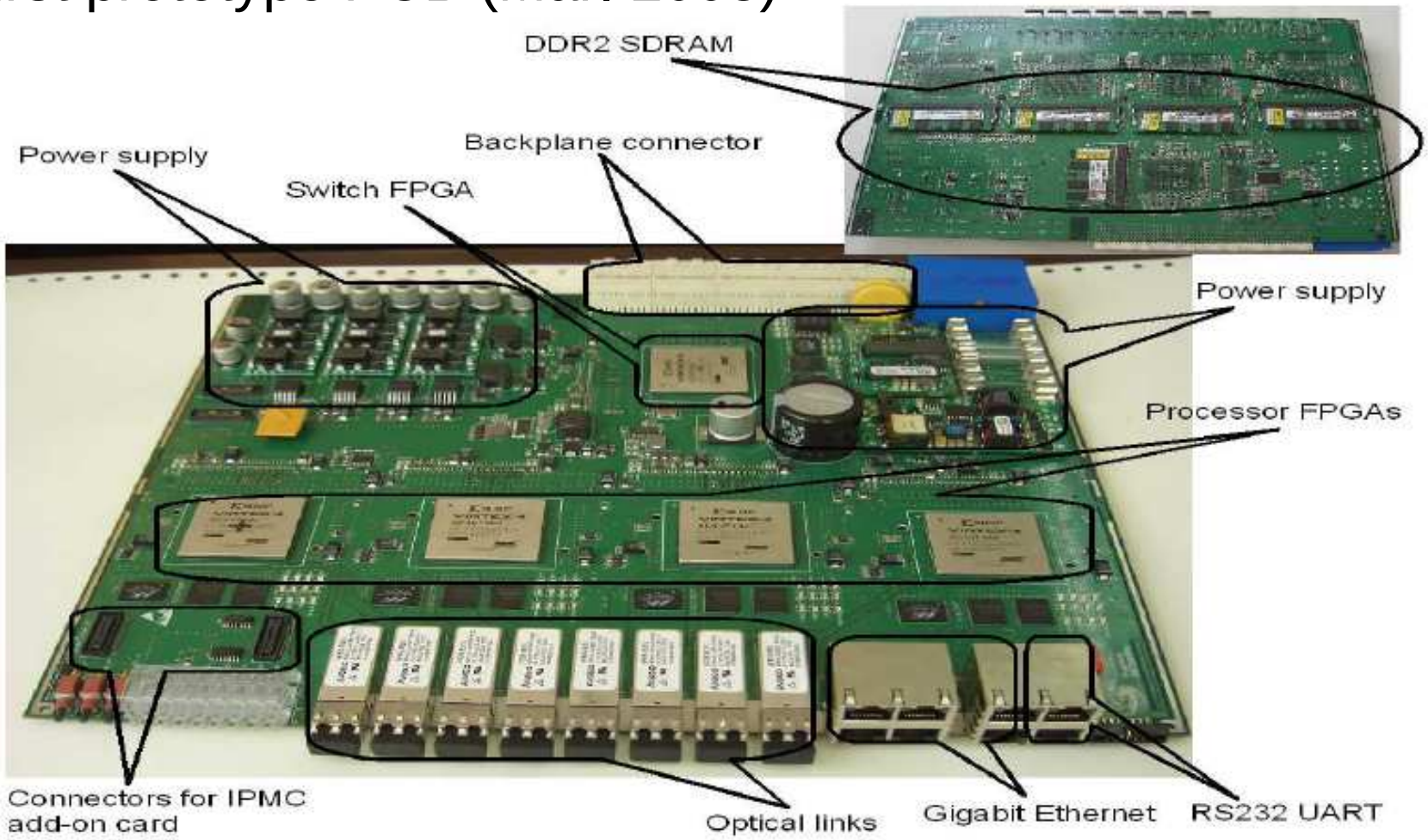




- ATCA based platform for online triggering
- Full-mesh topology of 14 CNs in one shelf
- CN design with 5 Xilinx Virtex-4 FX60 FPGAs
- 4 processor FPGAs + 1 switch FPGA
- 2 GB DDR2 memory per FPGA
- Optical links + Ethernet + peripherals

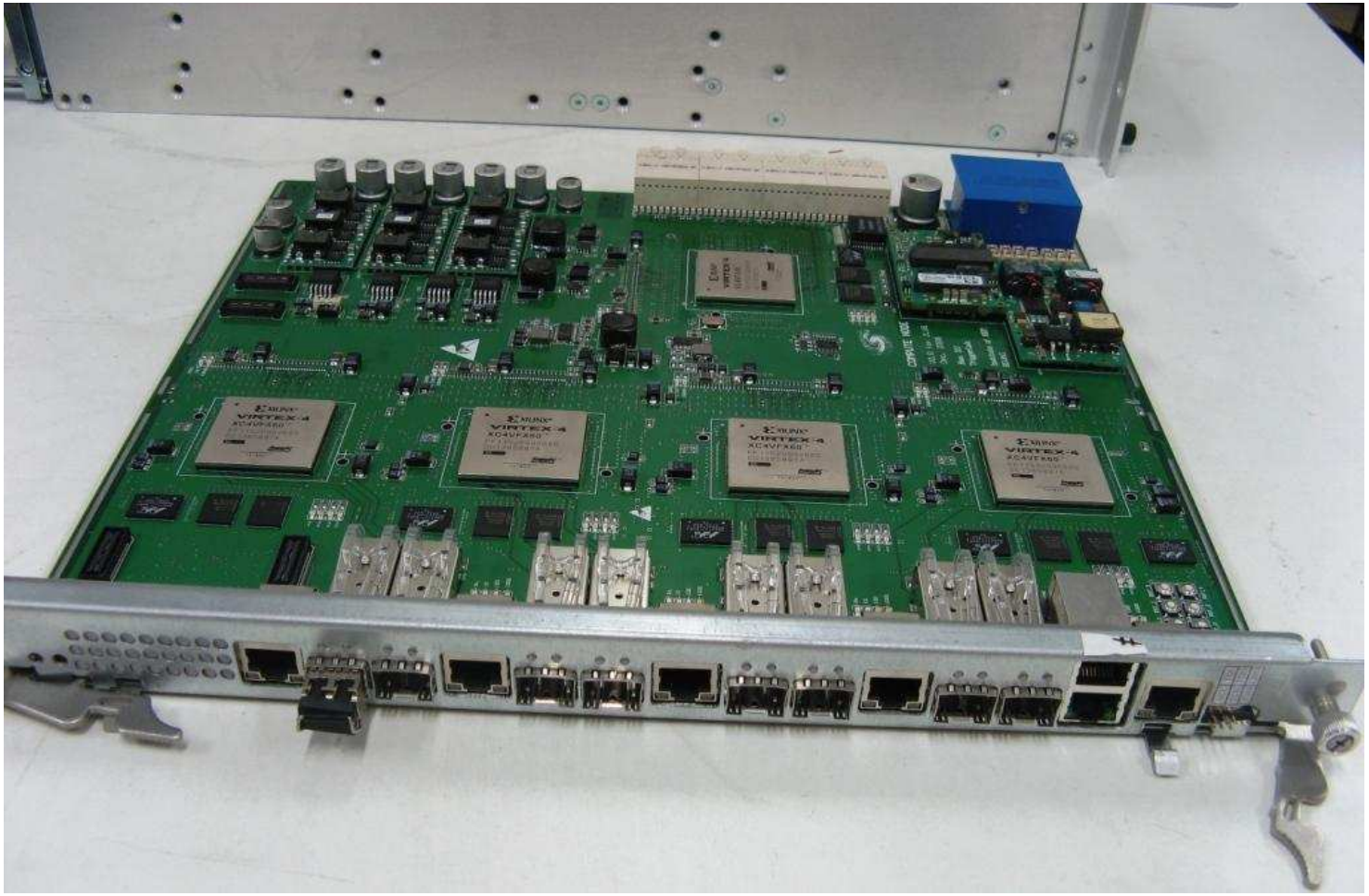
Compute Node HW Design

- First prototype PCB (Mar. 2008)

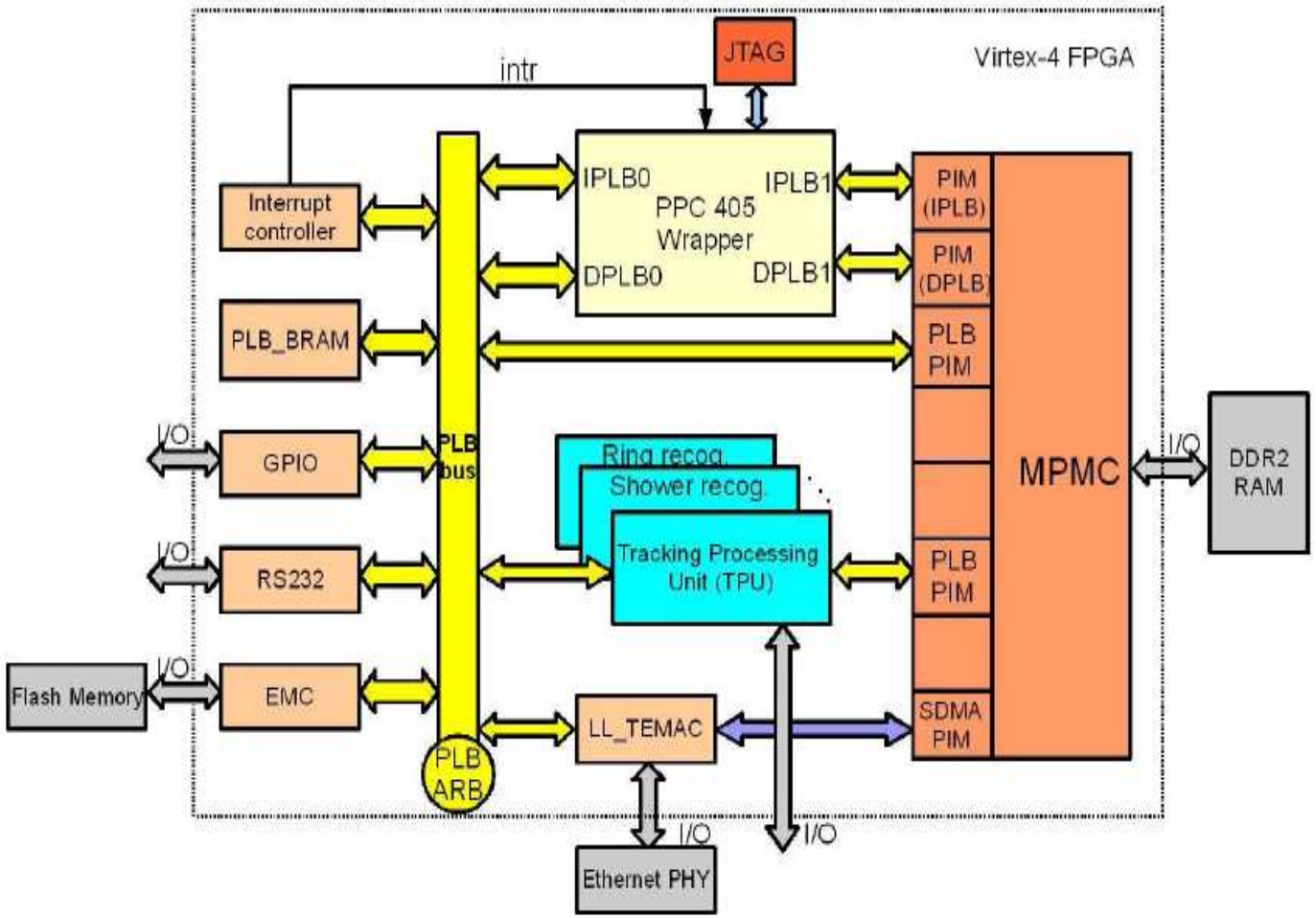


Compute Node HW Design

- Latest version PCB (Apr. 2009)

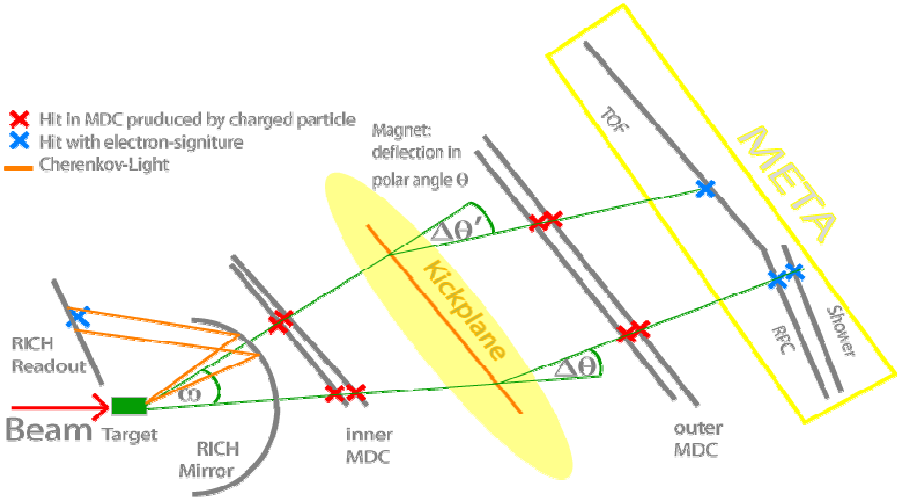


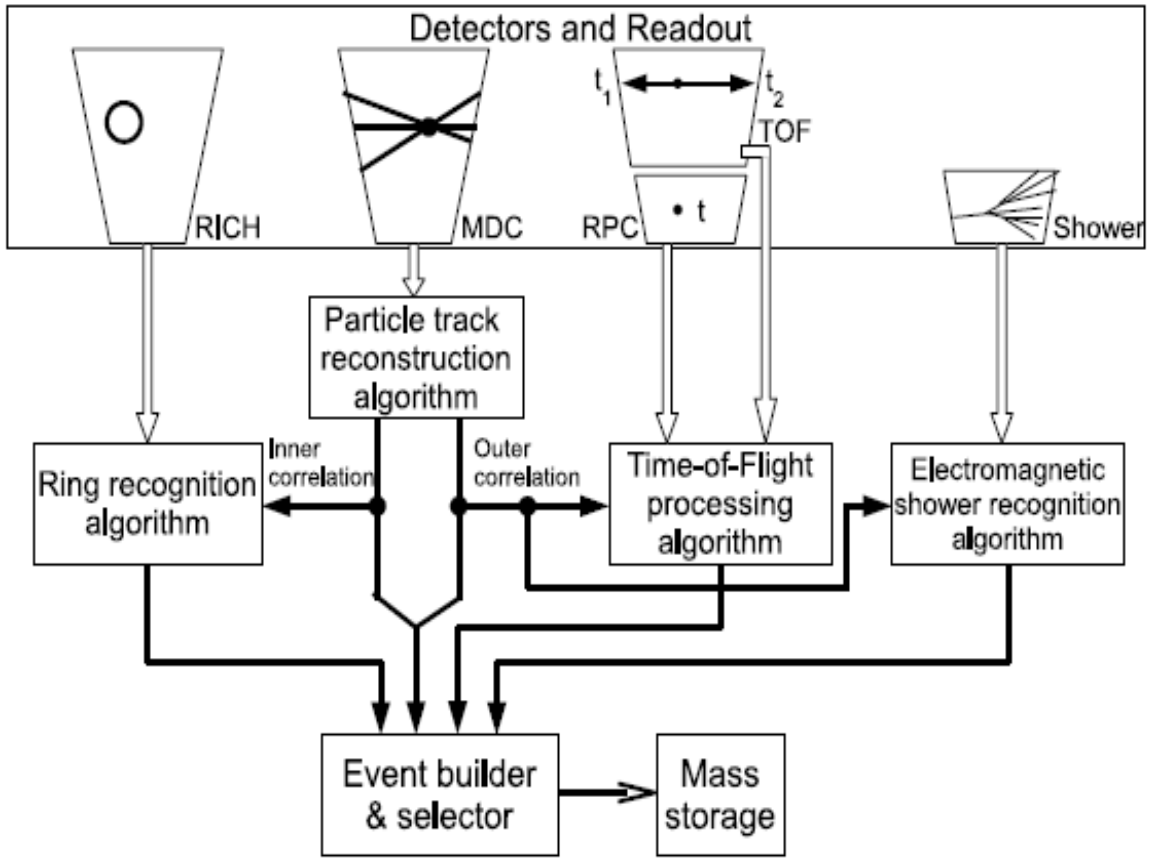
FPGA Design



- A uniform system design for all applications (PPC & MPMC based)
- Linux OS on PPCs
- Customized processing modules for detector-specific algorithms
- Easy system integration with the guarantee of high performance

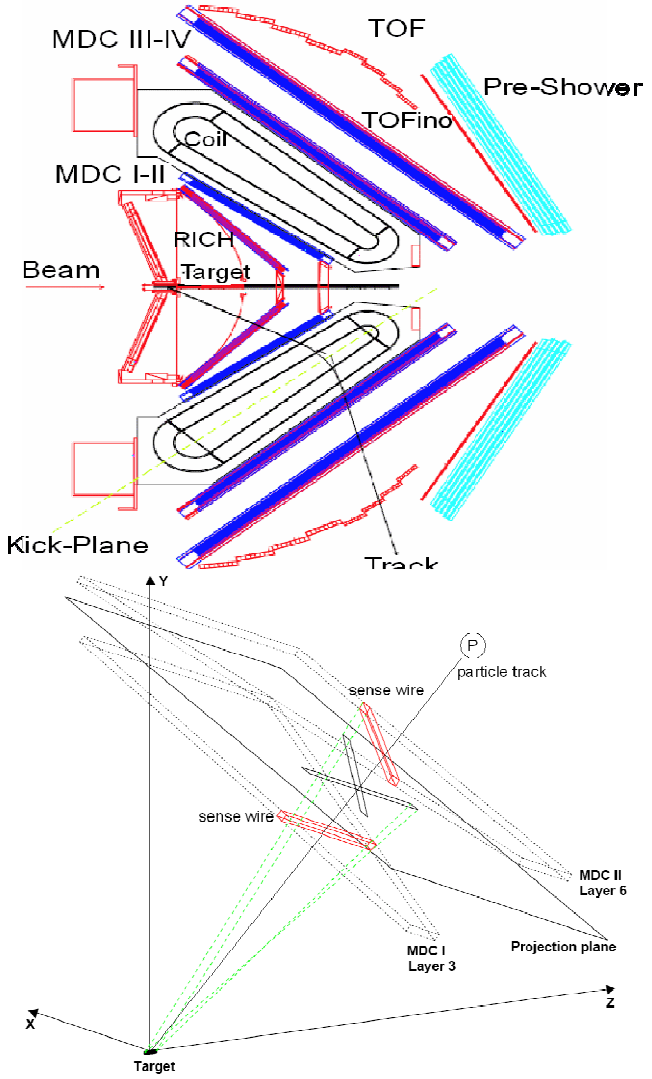
Algorithm Development

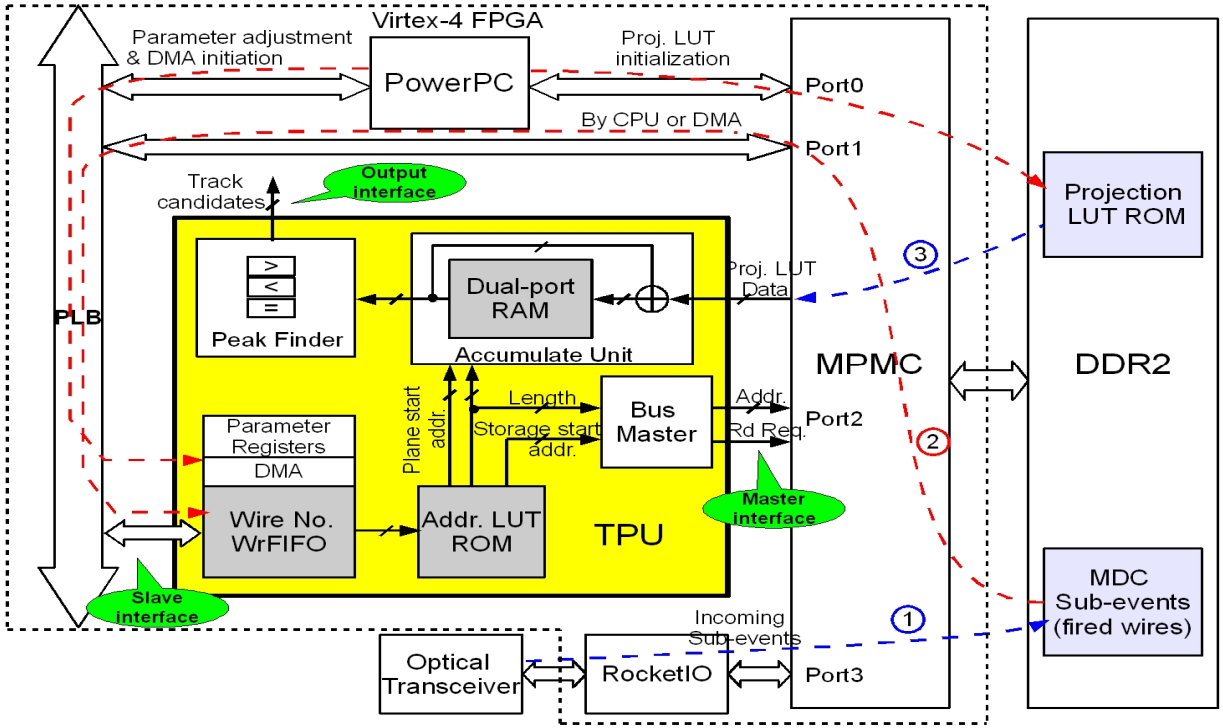




- Algorithms (for RICH, MDC, TOF, RPC, Shower detectors)
- HW implementation on FPGAs
- Correlations
  - RICH ~ Inner MDC (inner)
  - Outer MDC ~ TOF/Shower
- Event building & mass storage

MDC Tracking Algorithm



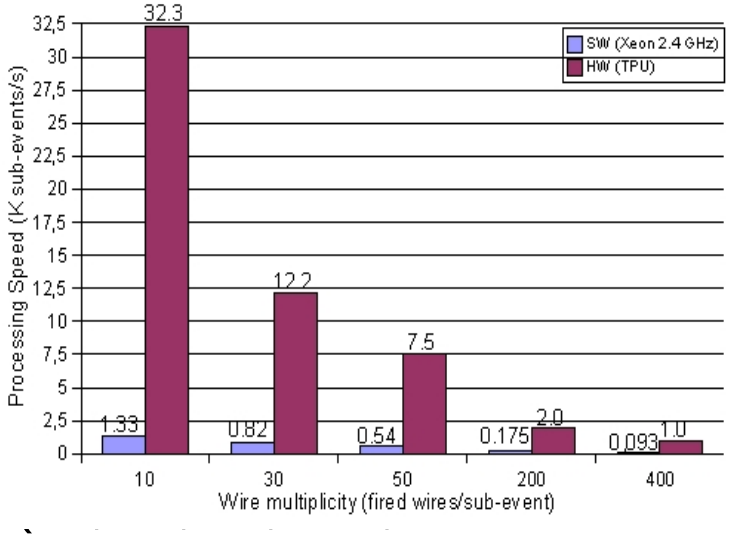


- Optical link for receiving incoming sub-events
- Tracking Processing Unit (TPU) for tracking
- DDR2 memory for sub-event buffering & LUT storage
- Memory-bounded computation
- Results to RICH Processing Unit (RPU) for correlation

MDC Tracking Algorithm

Experimental results:

- Resource utilization of V4 FX60 (<1/5) – acceptable!
- Timing limitation: 125 MHz without optimization
  - Clock fixed at 100 MHz, to match PLB & MPMC
- Processing capability measurements:
  - A C program running on the Xeon 2.4 GHz computer as SW reference
  - Measurement points on different wire multiplicities wires out of 2110)
  - Speedup of 10.8 – 24.3 times per module compared to the software solution
  - Multiple cores integrated on one FPGA for parallel processing (even higher performance speedup of two orders of magnitude)

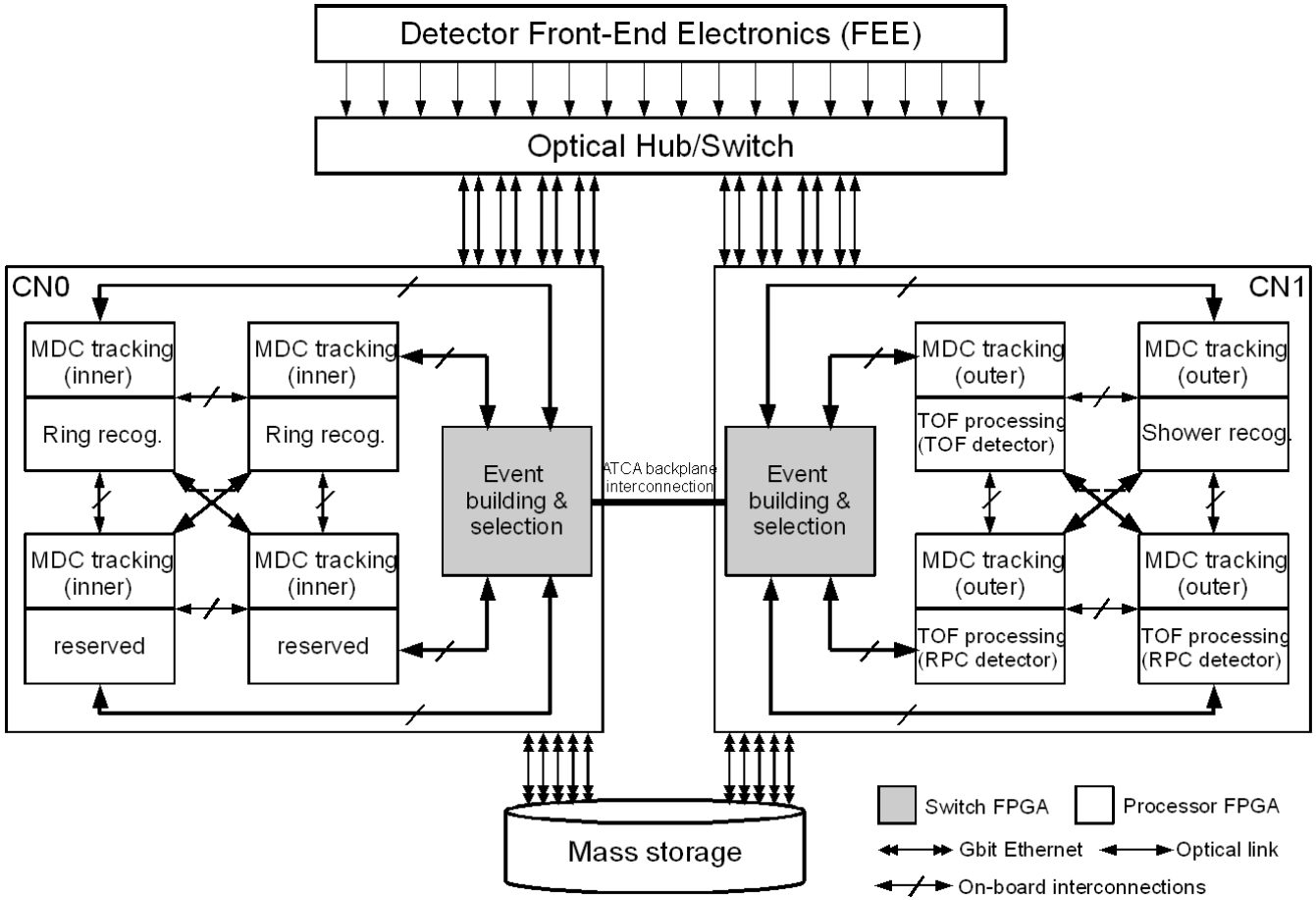


Other Algorithms for HADES

Except for the HADES MDC tracking, other algorithms are also being developed:

- Ring recognition for RICH (Johannes Roskoss, DPG'09, poster HK 67.105)
- TOF & electromagnetic shower processing (Andreas Kopp, DPG'09, poster HK 67.105)
- MDC outer tracking
- All algorithms are to be implemented on CNs for HW processing

Algorithm Partitions on CNs



- Max. 100 KHz reaction rate for HADES (100 KSub-events/s)
- 6 sectors (17 KSub-events/s per sector)
- 8 MDC tracking processors for each sector (4 inner & 4 outer)
- 2 CNs for each sector (12 + 1 CNs in one shelf for HADES)
- Algorithms evenly distributed on different FPGAs
- Correlations via on-chip, on-board, ATCA backplane interconnections

Current Status & Outlook

Currently:

- The first version CN PCB has been tested (no severe problem)
- The second version PCB is being tested in IHEP, Beijing.
- Algorithms under development & implementation

In the coming days:

- To finalize the PCB design and deliver for mass production
- ATCA connection investigation
- All algorithm implementations and distribution on FPGAs
- One ATCA crate for HADES with running algorithms (end of 2009, or beginning of 2010?)

Thanks for your attention!