JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

FPGA-based Adaptive Computing for Online Trigger Algorithms

Justus-Liebig-Universität Giessen

Ming Liu

for the HADES collaboration group

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Outline

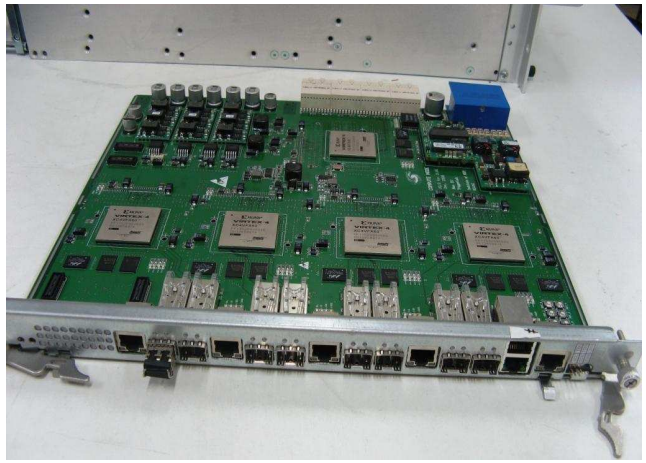
- Compute Node (CN) based DAQ & Trigger Systems
- FPGA Partial Reconfiguration (PR) Technology
- Adaptive Computing for Trigger Algorithms
- Current Status and Outlook

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

CN-based DAQ & Trigger System

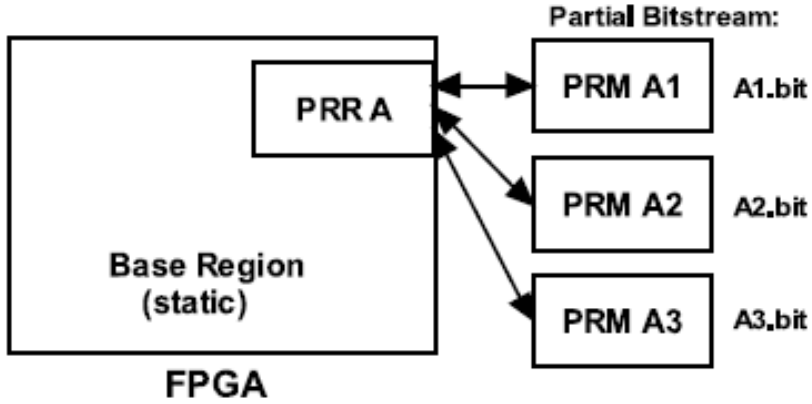
CN-based DAQ & trigger system for high-energy physics experiments:

- Xilinx Virtex-4 FX60 FPGA clusters
- ATCA interconnection architecture
- Optical links & Gigabit Ethernet
- Embedded hardcore PowerPCs & Linux OS on FPGAs
- Pattern recognition algorithms implemented as hardware co-processors (RICH ring recog., MDC tracking, TOF & Shower processing., …)
- A general-purpose computation platform for multiple experiments, such as HADES, PANDA, WASA, Belle2, …



Hardware Ready!!

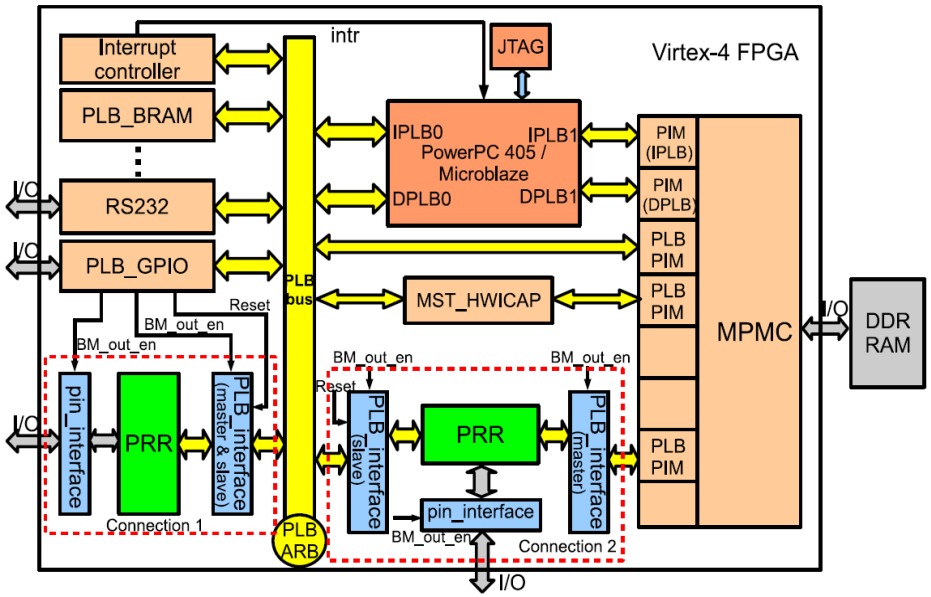
Partial Reconfiguration Technology

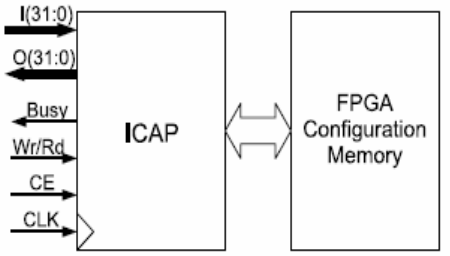


- PR Region (PRR) dynamically loaded with different design modules (partial bitstreams)
- Designs can be switched in the system run-time for different algorithms
- HW resources are multiplexed by different PR Modules (PRM)

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Partially Reconfigurable System

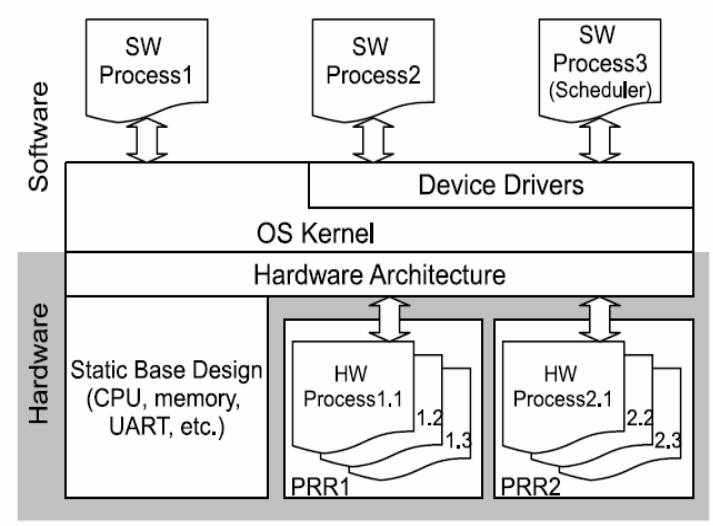




- PR region for algorithm modules
- Bus Macro interfaces to lock the routing between PRR & static design when implementation
- Run-time reconfiguration by ICAP (Internal Configuration Access Port)
- Dynamically load different PR Modules (PRM) by writing to ICAP

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Design Framework for Adaptive Computing



- A comprehensive framework in different HW/SW layers
  - HW PR design (static computer systems + reconfigurable algorithm modules as HW processes)
  - OS kernel for the base computer systems
  - Device drivers for algo. modules
  - Software scheduler for HW processes
- Reconfiguration speed is critical for performance
  - Module reconf. time in the order of magnitude of Micro-seconds (us), with our customized MST_HWICAP design
  - Reconf. time depending on design complexity

Adaptive Computing for online Triggering

Motivation:

- Multiple pattern recognition algorithms in DAQ & trigger systems (RICH ring recog., MDC tracking, TOF, Shower, …)
- Multiple cores for each algorithm for massive parallel processing
- Computation steps distributed on FPGAs
- Difficult to manage and modify the large system (many FPGAs, many algorithms, many cores, different FPGA bitstreams, long design synthesis & implementation time, …)
- Different computation features for algorithms (computation-bounded, memory-bounded, …)
- Traditionally all partitions are considered by designers during system development process -- NEITHER flexible, NOR efficient!!!

Adaptive Computing for online Triggering

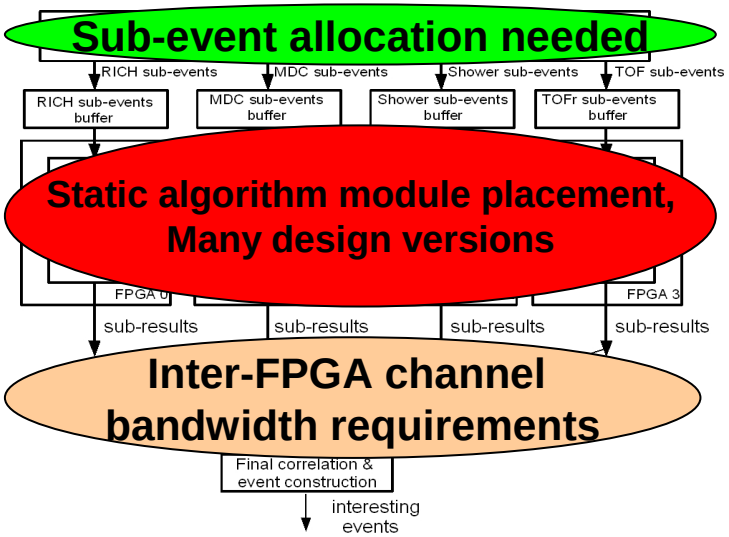
One promising solution: Adaptive computing

- Algorithm cores designed as PR modules
- Modules can be adaptively loaded during experiments, according to external factors (workload, sub-event types, …)
- Uniform DAQ & trigger design to interface with optical hubs, which delivers all kinds of sub-events
- Performance improvement due to the balance of computation and memory accesses, as well as more efficient utilization of FPGA resources?
- Other merits?... (to be explored)

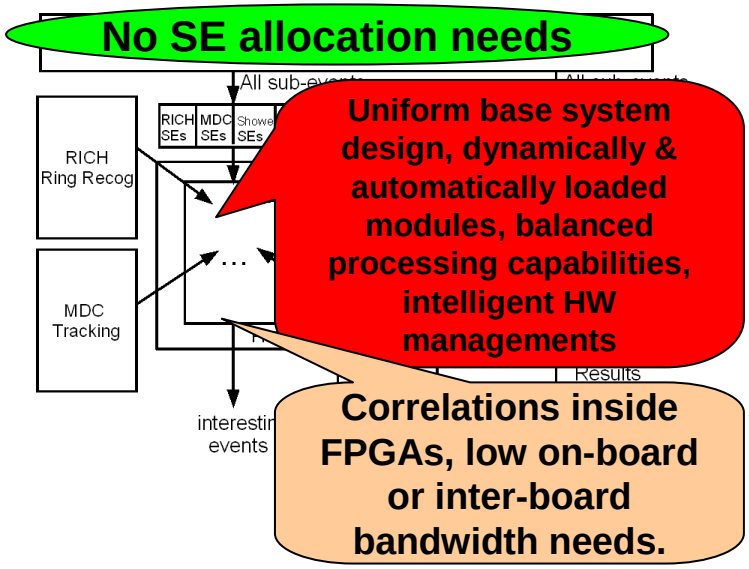
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Comparison

Traditional non-PR design:



PR design for adaptive computing:



- No data distribution requirements for optical hubs (all kinds of sub-events fed into all FPGAs)
- Uniform design in adaptive computing – easy to maintain system designs
- Balanced computing and more efficient FPGA resource utilization

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Current Status and Outlook

At present:

- CN PCB is ready for mass production.
- The design framework for adaptive triggering has been architecturally constructed.
- MDC inner tracking has been ported on the FPGA and evaluated.

In the future:

- Trigger algorithms for RICH, outer MDCs, TOF, Shower are to be implemented on FPGAs. (two more master theses)
- The adaptive design framework is to be elaborated in different aspects.
- Real algorithm cores are to be applied for adaptive triggering.

Thanks for your attention!