# CMIT- A Novel Cluster-based Topology for 3D Stacked Architectures

Masoud Daneshtalab, Masoumeh Ebrahimi, Pasi Liljeberg, Juha Plosila, Hannu Tenhunen
*Department of Information Technology, University of Turku, Finland*
*{ masdan, masebr, pakrli, juplos, hanten }@utu.fi*

***Abstract- Combining the benefits of 3D IC and Network-on-Chip (NoC) schemes, provides a significant performance gain for 3D stacked architectures. In recent years, Through-Silicon-Via (TSV), employed for inter-layer connectivity (vertical channel), has attracted a lot of interest since it enables faster and more power efficient inter-layer communication across multiple stacked layers. However, the area overhead of TSVs reduces wafer utilization and yield which impact design of 3D architectures using a large number of TSVs. In this paper, we propose a novel stacked topology, named CMIT (Cluster Mesh Inter-layer Topology) for 3D architectures to reduce the area overhead of TSVs and power dissipation on each layer with minimal performance penalty. Experimental results with synthetic test cases demonstrate that the presented topology can save more than 75% of TSV area footprint and reduces more than 10% of power consumption with a negligible performance overhead.***

## I. INTRODUCTION

The Three Dimensional (3D) integration has emerged as a potent solution to address the design complexity of Multi Processor Systems-on-Chips (MPSoCs) in 2D Integrated Circuits (IC). 3D ICs reduce the interconnect delay problem by stacking vertically active silicon layers as well as offering a number of advantages over the traditional 2D chip [1][2][3][4]: (1) shorter global interconnects; (2) higher performance; (3) lower interconnect power consumption due to wire-length reduction; (4) higher packing density and smaller footprint; and (5) support for the implementation of mixed-technology chips.

3D NoC topologies not only create scalable networks to address communication requirements in 3D ICs [1]-[4] but also are a crucial factor of 3D chips in terms of performance, cost, and energy consumption [1]. Various on-chip network topologies have been studied for 3D NoCs [1]-[5][6][7][9]. Mesh-based structures are popularly used in 3D systems, because their grid-based regular structure is intuitively considered to be matched to the 2D VLSI layout for each stack layer [1][2][3][4][6]. Nevertheless, if the number of IP-cores and memories increases in each layer, more TSVs are necessitated to handle the inter-layer communication. Inasmuch as each TSV employs a pad for bonding, the area footprint of TSVs in each layer is augmented significantly [4][9].

In this paper, we propose a novel stacked mesh topology to reduce the area overhead of TSVs and power dissipation with minimal performance penalty. The proposed stacked mesh topology, named Clustered Mesh Inter-layer Topology (CMIT), benefits of clustering the mesh topology for each layer. Each cluster of the presented topology has its dedicated vertical channel, composed of a set of TSVs. CMIT preserves the advantages of the clustered mesh topology and mitigates both power density and TSVs area footprint on each layer.

The rest of the paper is organized as follows. In Section 2, the background is discussed. In Section 3, a brief review of related works is presented while the proposed topology is presented in Section 4. The experimental results are discussed in Section 5 with the summary and conclusion given in the last section.

## II. BACKGROUND

### A. 3D IC Technology Overview

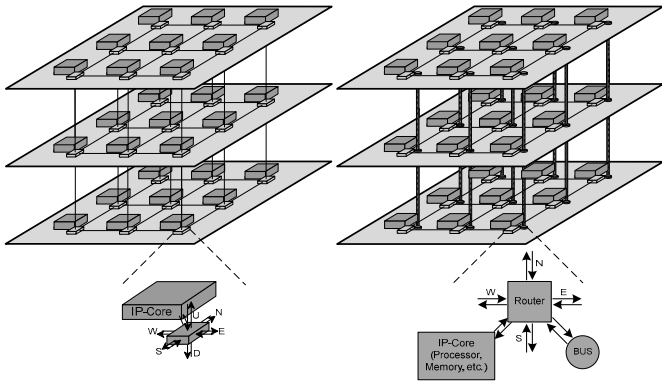
There are many technologies for die stacking being pursued by industry and academia. Wafer-Bonding [10] and Multi-Layer Buried Structures (MLBS) [11] are the most promising ones. Wafer-to-wafer bonding appears to be the leading contender in industry and many recent academic studies have assumed this type of 3D stacking technology [1]-[5][12]. Wafers can be stacked either Face-to-Face (F2F) or Face-to-Back (F2B) and both have pros and cons. While the former provides the greatest layer-to-layer via density, it is suitable for two layers; additional layers would have to employ back-to-back placement using larger and longer vias. On the other hand, F2B provides uniform scalability to an arbitrary number of layers, despite a reduced inter-layer via density [7]-[13]. Layers, stacked on top of each other, are connected via vertical interconnects tunnelling through them. Wire bonding, micro-bump, contactless, and TSV are some of the vertical interconnect technologies that have been used in stacked structures [11]. The TSV interconnection has the potential to offer the greatest vertical interconnect density and therefore is the most promising one among these vertical interconnect technologies [7]-[13]. In this work, we assume the F2B method with TSV interconnects to provide more scalability when more than two layers are employed.

### B. 3D NoC Architecture

3D-Symmetric NoC and 3D NoC-Bus Hybrid (stacked mesh) structures are popularly used in 3D systems, because their grid-based regular structure is intuitively considered to be matched to the 2D VLSI layout for each stack layer [1][2][3][4][6]. The 3D-symmetric NoC structure, shown in Fig. 1(a), is an extension of 2D mesh by adding two additional physical ports to each baseline-router (one for up and one for down) in the popular 2D mesh-based system[1][4]. Adding two additional ports requires larger crossbar incurring significant area and power overhead and increases the blocking probability inside the router. Since TSVs are relatively shorter and wider than that of intra-layer interconnects, they have low resistance

and can support higher signalling speeds [4][9]. As router latencies may dominate the throughput of fast vertical interconnects, this has led the researchers to propose the 3D NoC-Bus Hybrid structure using a bus with a centralized arbiter for each vertical channel, which allows single hop latency for packets between any number of layers [1]-[4]. As depicted in Fig. 1(b), on-chip routers in this structure have at most 6 ports, one to the IP-core, one to the bus, and four for cardinal directions. According to [4] the 3D hybrid structure was observed to be more efficient than the 3D symmetric for the vertical interconnection as long as the number of device layers was less than 9. Thus, in this work we take advantage of 3D hybrid structure.

Nonetheless, a relatively high area penalty due to via blockage may impose limitations on the number of TSVs that can be utilized for inter-layer communication [4][9][14]. Indeed, not only the area overhead of TSVs is quite high, but also floor planning and routing is also extremely challenging since TSVs are distributed in each layer. In this work, we present two area-efficient stacked architectures to reduce the TSV footprint with minimal performance overhead.




(a) (b)

Fig. 1. Mesh-based NoC architectures: (a) 3D-symmetric NoC (b) 3D NoC-Bus Hybrid structures

## III. RELATED WORK

Design techniques and methodologies for 3D architectures have been investigated to efficiently exploit the benefits of 3D technologies. Several NoC topologies for 3D systems have been exhaustively investigated in [1]-[4][7][15]. The authors in [1] demonstrate that besides reducing the footprint in a fabricated design, 3D systems provide more efficient performance than 2D systems. They have also demonstrated that both mesh and tree topologies for 3D systems achieve more efficient performance compared to traditional 2D systems. However, the mesh topology shows significant performance gains in terms of throughput, average latency, and energy dissipation with a small area overhead [1]. In [15] different 3D mesh-based architectures have been compared in the zero-load latency, but the performance of the network with different traffic patterns and loads is also necessary to be evaluated. To form an optimistic 3D mesh-based system, several 3D structures have been presented. Baseline-routers in 2D mesh-based systems have 5 ports, i.e. 4 ports to adjacent routers and one for the resource node. The straightforward extension for 3D mesh-based systems (3D-symmetric NoC) is to utilize routers with two additional inter-layer links by adding two physical ports to baseline-routers (one for up and one for down) [1][4][6][7][16]. As mentioned earlier, the 3D structure using such routers, not only increases the area and power overhead of the routers but also contention in the routers may arise. The electrical behaviour of the relatively short and wide TSVs, i.e. the low resistance, and supporting much higher signalling speeds led the authors of [4] to propose the 3D-hybrid structure. This 3D structure exploits the dynamic Time Division Multiple Access (dTDMA) bus [17][18] with a centralized arbiter for the vertical communication link. Thus, moving from one layer to any of the other layers takes only one hop. However, contention issues in the bus limit the attainable performance gains [1]. That is, such structures inherently suffer from the weakness of buses since only one transmission is allowed each time over a vertical bus.

To reduce the area footprint of TSVs, a serialization scheme for vertical channels has been presented in [9], but this scheme is only applicable with the 3D-hybrid structure where each node has a dedicated vertical channel.

Due to the above concerns, in this paper, we have focused on both the 3D-symmetric structure and the 3D-hybrid structure. Our proposed stacked architectures, are applicable for both 3D-hybrid and 3D-symmetric structures and, in addition to that, a group of nodes share a vertical channel as inter-layer interconnection.

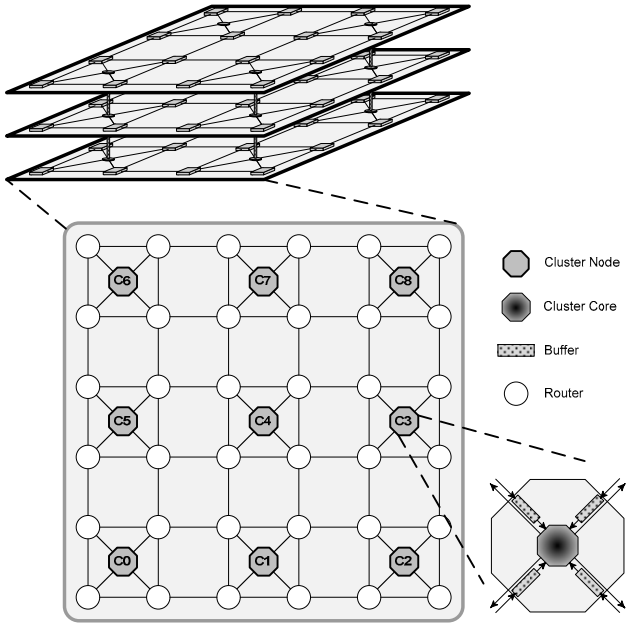



Fig. 2. The CMIT network.

## IV. CMIT (CLUSTER MESH INTER-LAYER TOPOLOGY)

The structure of CMIT, depicted in Fig. 2, is basically similar to that of the mesh topology, except that for every layer the number of vertical channels has been reduced by sharing a vertical bus among routers of each cluster. That is, even preserving the advantage of the mesh on each layer, CMIT diminishes the number of inter-layer interconnections to meet constraints on the number of TSVs. In CMIT, each node (IP-core/memory) is connected to a router having at most 6 ports: one to the node, one to the bus, and four for the neighbors. Fig.

2 exhibits CMIT with 36 nodes, in which every four routers are grouped into a cluster on each layer. Even though CMIT achieves better area and power efficiency than the typical 3D mesh structure due to reducing the number of vertical channels, since several routers are connected to a shared vertical bus, the performance can be degraded when the inter-layer traffic is augmented. The arbiter should be placed in the middle layer of the chip to keep wire lengths as uniform as possible. The number of control wires of each arbiter increases with the number of nodes attached to the vertical channel (bus). As a result, the presence of a centralized arbiter is one of the reason why the number of vertical channels in the chip should be kept low [4][9]. We believe that, the proposed topology can keep the number of vertical channels low with a negligible performance penalty.

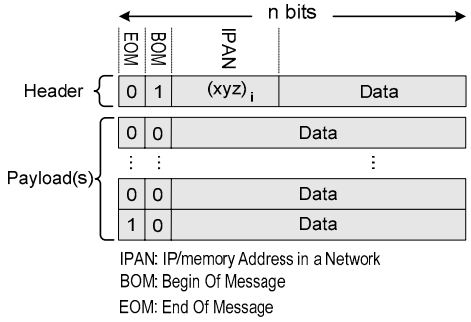



Fig. 3. The packet format of CMIT.

### A. Routing Algorithm

For the presented CMIT, we employ the dimension order routing (DOR) algorithm which guarantees the network is deadlock free. DOR is a minimal deterministic routing in which the message is first forwarded along the X-dimension, then along the Y-dimension, and, finally, along the Z-dimension. Fig. 3 shows the packet format of the CMIT network. The header flit is $n$ bit wide and the $n^{th}$ bit is the EOM (End Of Message) sign and the $(n-1)^{th}$ bit is the BOM (Begin Of Message) sign. The third field (i.e. IPAN) indicates the address of the destination address of an IP-core/memory node inside the cluster node. The content of the message is located in the rest of the flits (Payload). In CMIT the routing is performed by typical routers. That is, cluster routers are only employed for the purpose of inter-layer communication in CMIT.

## V. Experimental Results

In this section, we compare the presented topology with the conventional structures in terms of latency, power consumption, and area cost. A 3D NoC simulator is implemented with VHDL to assess the efficiency of the proposed architectures. The simulator models all major components of the NoC such as network interfaces, routers, and wires along with vertical channels.

### A. System Configuration

We configure a 64-node (4×4×4) 3D stacked architecture. In this configuration, illustrated in Fig. 4, out of 64 nodes, 16 nodes are assumed to be processors and other 48 nodes are memories, i.e. DRAMs. The processors are 32b AXI and the memories are DDR2-512MB (tRP-tRCD-tCL=2-2-2, 32b, 4 banks) [19]. In addition, two different 3D on-chip network topologies are considered for the experiment: 3D hybrid structure and CMIT. The 3D hybrid and CMIT networks are formed by a typical state-of-the-art router structure including input buffers, a VC (Virtual Channel) allocator, a routing unit, a switch allocator, and a crossbar as well as an interface unit connecting the router to either a vertical channel (bus) or a cluster router. Typical routers of 3D hybrid and CMIT have at most six input/output ports. Every cluster router of CMIT has five input/output ports, i.e. four for local routers and one for the vertical channel interface. Each input port of the routers has two VCs where packets of different message types (request and response) are assigned to corresponding VCs to avoid message dependency deadlock [20]. The arbitration scheme of the switch allocator in the typical router structure is round-robin. The array size, routing algorithm, link width, number of VCs, buffer depth of each VC, and traffic type are the other parameters which must be specified for the simulator. The routers adopt the DOR routing and utilize wormhole switching. For all routers, the data width (flit) was set to 32 bits, and the buffer depth of each VC is five flits. As mentioned earlier, to compensate the performance loss due to using the bus as the vertical interconnect, each vertical channel is composed of two unidirectional channels in opposite directions to propagate the inter-layer data. Thus, 32 bits of the channel is allocated to upward direction and the other 32 bits of the channel is employed for the downward direction. Each direction has its arbiter module and bus controller based on the dTDMA bus structure [4][17]. The presented configuration uses one flit for messages related to read requests and write responses, and the size of read request messages typically depends on the network size and memory capacity of the configured system. The message size of the read responses and write requests is variable and depends on the request/response length produced by a master/slave core. As the performance metric, we use latency defined as the number of cycles between the initiation of a request operation issued by a master (processor) and the time when the response is completely delivered to the master from a slave (memory). The request rate is defined as the ratio of the successful read/write request injections into the network interface over the total number of injection attempts. All the cores and routers are assumed to operate at 1 GHz. For fair comparison, we keep the bisection bandwidth constant in all configurations. All memories (slave cores) can be accessed simultaneously by each master core continuously generating memory requests. To estimate the power consumption of networks, we have used Orion library functions [21] as well as the power and delay values of vertical links in [15].

### B. Physical Analysis

To compute the network area for each topology, we estimate the area of routers, cluster routers, and vertical channels. The network platform of each topology with the aforementioned configuration is synthesized with Synopsys Design Compiler using the UMC 0.09µm technology. In this work, the pad size for TSVs is assumed to be 5µm square with pitch of around 8µ, the flit-width is set to 32 bits, and each vertical channel requires 3×14 control wires for arbitration in a four stacked layer [4]. After the TSV area is calculated with the given values, the TSV footprint has been reduced from 0.41 $mm^2$ in 3D hybrid to 0.1 $mm^2$ in CMIT, resulting in about 75% area saving for TSV footprint.

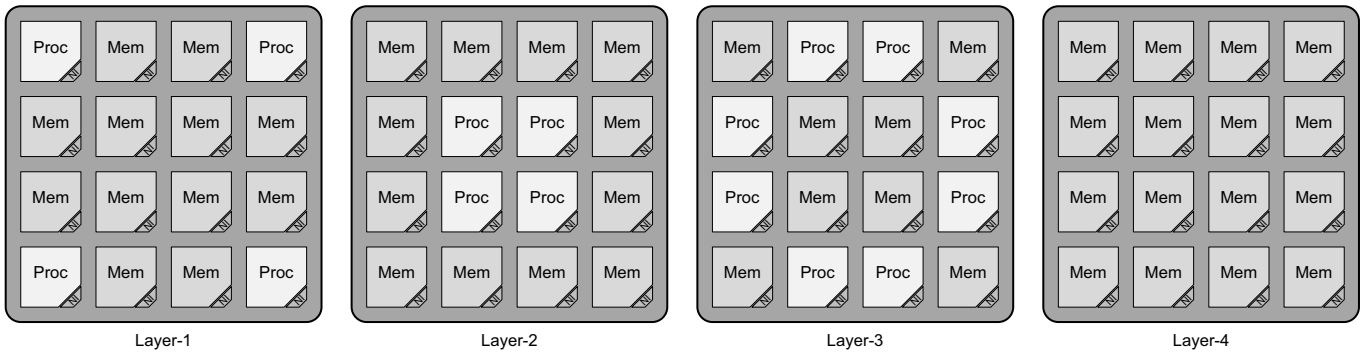



Fig. 4. 4×4×4 stacked mesh layout.

Also, 3D hybrid occupies larger network area compared with CMIT, because each router in 3D hybrid has a compact transceiver module to interface with the vertical channel (bus) and each bus should have its own arbiter module. Likewise 3D hybrid, in CMIT the transceiver and arbiter modules are only integrated in cluster routers so that the total network area used by CMIT is 10% lower than that of 3D hybrid.

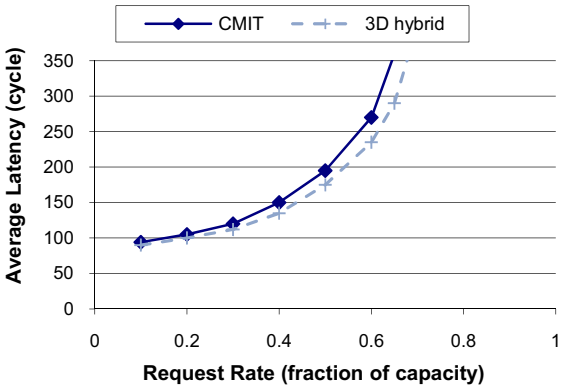



Fig. 5. Performance under the uniform traffic profiles.

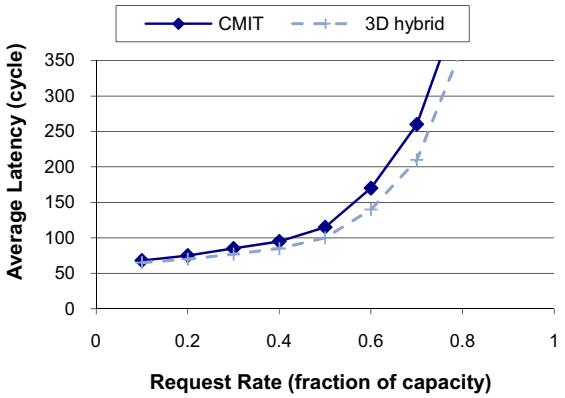



Fig. 6. Performance under the non-uniform traffic profiles.

## C. *Performance Analysis*

To assess the performance of the presented topology, the uniform and non-uniform synthetic traffic patterns have been considered separately. The random traffic represents the most generic case, where each processor sends in-order read/write requests to memories with the uniform probability, and the memories and request type (read or write) are selected randomly. Eight burst sizes, from 1 to 8, are stochastically chosen according to the data length of the request. In the non-uniform mode, 70% of the traffic is local requests, where the destination memory is one hop away from the master core, and the rest 30% of the traffic is uniformly distributed to the non-local memory modules.

Fig. 5 and Fig. 6 show the simulation results under the uniform and non-uniform traffic profiles, respectively. As demonstrated in both figures, 3D hybrid has lower average latency than CMIT. This is because the number of inter-layer channels in CMIT is lower than that of 3D hybrid structure. Therefore, the traffic in CMIT vertical channels is higher than that of the 3D hybrid structure. The average latency of each structure has been computed near saturation point (0.5) under the non-uniform traffic profile. As a result, the average latency of CMIT is 11% higher than that of the 3D hybrid. That is, the performance penalty of CMIT is around 11%, while it saves 75% of TSVs area.

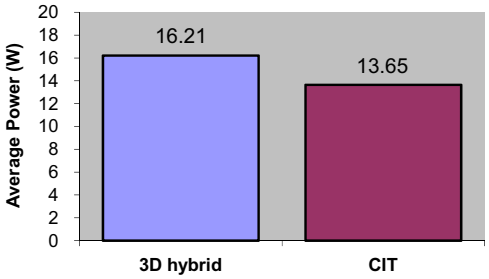



Fig. 7. Average power dissipation results under uniform traffic profile.

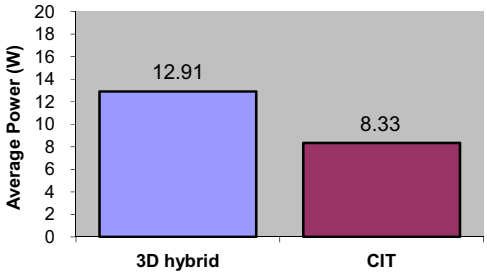



Fig. 8. Average power dissipation results under non-uniform traffic profile.

### D. Power Analysis

Using the simulator, the average power consumption of the presented topology was calculated and compared under uniform and non-uniform traffic patterns close to the saturation point. The results for the average power consumption under uniform and non-uniform are shown in Fig. 7 and Fig. 8. According to Fig. 5 and Fig. 6, the saturation points that have been considered for computing the average power consumption values are 0.3 for uniform traffic and 0.5 for non-uniform traffic. As the results presented in Fig. 7, the average power dissipation of the network formed by CMIT is 6% lower than that of the 3D hybrid scheme under the uniform traffic profile. The results of Fig. 8 indicate that the average power consumption of CMIT is 10% lower than that of the 3D hybrid scheme under the non-uniform traffic profile. We can notice that although cluster routers are not implemented in the 3D hybrid structure, but because in 3D hybrid there is a separate dTDMA bus module with large central arbiter is integrated for each node, 3D hybrid consumes more power and has area overhead compared to CMIT. The bus modules are only integrated in cluster routers in the CMIT network.

## VI. CONCLUSION

3D stacked architectures provide significant benefits in performance and footprint. It has also been demonstrated that combining 3D ICs and on-chip networks can be a promising option for designing large multiprocessor architectures. One critical issue in 3D design is that the vertical interconnections are very fast and fat such that the area overhead of TSVs impose constraints on the number of TSVs for existing 3D architectures. Since the area overhead of TSVs imposes constraints on the number of TSVs for existing 3D architectures, a novel topology has been presented to deal with constraints on the number of TSVs. Experimental results have revealed that the proposed topology not only reduces the number of TSVs significantly but also diminishes the power consumption with low performance penalty.

## ACKNOWLEDGMENT

The authors wish to acknowledge the academy of Finland and Nokia Foundation for the financial support during the course of this research.

## REFERENCES

[1] B. S. Feero, P. P. Pande, "Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation," IEEE Transactions on Computers, vol. 58, no. 1, pp. 32-45, Jan. 2009.

[2] D. Park, S. Eachempati, R. Das, A. K. Mishra, Y. Xie, N. Vijaykrishnan, and C. R. Das, "MIRA: A Multi-Layered On-Chip Interconnect Router Architecture", ISCA 2008, pp. 251-261, Pennsylvania State, USA.

[3] J. Kim, C. Nicopoulos, D. Park, R. Das, Y. Xie, V. Narayanan, and C. R. Das, "A novel dimensionally-decomposed router for on chip communication in 3D architectures," in Proc. of the ISCA, pp. 138-149, Boston, USA, 2007.

[4] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, and M. Kandemir, "Design and Management of 3D Chip Multiprocessors Using Network-in-Memory," In 33rd International Symposium on Computer Architecture (ISCA), pp. 130–141, 2006.

[5] I. Loi and L. Benini, "An Efficient Distributed Memory Interface for Many-Core Platform with 3D Stacked DRAM," in Proc. of the DATE Conference, Germany, pp. 99-104, 2010.

[6] I. Loi, F. Angiolini, L. Benini, "Supporting vertical links for 3D networks on chip: toward an automated design and analysis flow," in Proc. Nanonets, 2007.

[7] A. Y. Weldezion et al., "Scalability of the Network-on-Chip communication architecture for 3D meshes," In proc. NoCS, pp. 114-123,2009.

[8] I. Savidis et al., "Electrical modeling and characterization of through-silicon vias (TSVs) for 3D integrated circuits," Microelectronics Journal, Vol. 41(1), pp. 9-16, 2010.

[9] S. Pasricha, "Exploring Serial Vertical Interconnects for 3D ICs," in Proc. IEEE/ACM DAC, pp. 581-586, 2009.

[10] S. Das et al., "Technology, Performance, and Computer Aided Design of Three-Dimensional Integrated Circuits," In Proc. International Symposium on Physical Design, USA, pp. 108-115, 2004.

[11] Y. Xie, G. H. Loh, B. Black, K. Bernstein, "Design Space Exploration for 3D Architectures," ACM Journal on Emerging Technologies in Computing Systems 2, pp. 65–103, 2006.

[12] B. Black et al., "Die-Stacking (3D) Microarchitecture," in Proceedings of MICRO-39, pp. 469-479, 2006.

[13] G. H. Loh, "3D-Stacked Memory Architectures for Multi-core Processors," in proc. of International Symposium on Computer Architecture (ISCA), pp. 453–464, 2008.

[14] M. Grange et al., "Physical mapping and performance study of a multi-clock 3-Dimensional Network-on-Chip mesh", in Proc. IEEE International Conference on 3D System Integration (3D IC), 2009, San Francisco, USA, pp. 1-7, 2009.

[15] V.F. Pavlidis et al., "3D Topologies for Networks-on-Chip," IEEE Transactions on Very Large Scale Integration Systems, 15(10):1081, 2007.

[16] S. Murali et al., "Synthesis of networks on chips for 3D systems on chips," In Proc. of ASPDAC'09, pp. 242-247, Jan. 2009.

[17] T. Richardson et al. "A hybrid SoC interconnect with dynamic TDMA-based transaction-less buses and on-chip networks", In Proc. VLSID, pp. 8-15, 2006.

[18] A. Y. Weldezion et al., "3D Memory Organization and Performance Analysis for Multi-processor Network-On-Chip Architecture," in Proc. of IEEE International 3D System Integration Conference (3D-IC), San Francisco, USA, 2009.

[19] Micron Technology, Inc. Micron 512Mb: x4, x8, x16 DDR2 SDRAM Datasheet, 2006.

[20] S. Murali, and et al. "Designing message-dependent deadlock free networks on chips for application-specific systems on chips," In Proc. VLSI-SoC, pages 158-163, 2006.

[21] A. Kahng et al., "Orion 2.0: A fast and accurate noc power and area model for early-stage design space exploration," in proc. of DATE, pp. 423-428, 2009.