SRAM Gauge: SRAM Health Monitoring via Cells Race

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***Abstract*—By shrinking transistors' dimensions and, consequently, reducing the operating voltage in nano-scale CMOS technologies, the stability of SRAM cells has become a major reliability concern. SRAM cells' robustness against undesirable bit-flips is commonly measured by Static Noise Margin (SNM). Degradation in SNM is mainly because of the gradual variations in transistors' parameters due to aging. This work proposes a built-in SRAM health sensor capable of monitoring the SNM of individual SRAM cells in a memory block. The sensor is composed of extra non-operational sensor cells with different predefined SNMs. These sensor cells are put in a race with operational SRAM cells to determine their strength. The precision, sensing range, and robustness of the proposed sensor against process variation are adjustable at the cost of small area overhead. In our simulation setup, with the area overhead of 0.29%, the sensor monitors a wide range of SNMs from 275 mV to 325 mV, with a precision of 5 mV.**

I. Introduction

Deviation from transistors' nominal parameters due to aging is one of the main dependability challenges in nanoscale transistor fabrication [1–3]. Aging negatively affects the stability and performance of the chip, while increases the power consumption due to the need for a larger guard-band for operating voltage and frequency [2].

The leading causes of transistors' parameters drift over time are Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time-Dependent Dielectric Breakdown (TDDB), which are called aging [4–6]. At a constant operating voltage, aging reduces the drive current of transistors and gradually increases the absolute value of the threshold voltage (V_{th}). By shrinking transistors' dimensions, the electric field in the gate insulator, the current density in the transistor channel, and hot-spots are increased, accelerating the chip's aging rate [4, 7].

The Static Random Access Memory (SRAM) is the most susceptible component to aging in System-on-Chips and FPGAs [2, 7, 8]. Since a significant area of these chips is occupied by SRAM cells, monitoring the SRAM health state is essential to ensure a reliable system operation [7]. Monitoring also helps in better managing the power consumption.

The main effect of aging on SRAM cells is manifested as the reduction of Static Noise Margin (SNM) [7]. Other factors such as supply voltage drop, temperature fluctuations, and process variations (PV) also cause divergence in SNM of SRAM cells in a memory array. To monitor the aging state of SRAM memory, various aging sensors are presented in previous works. These works rely on some parameters such as current consumption of SRAM during different operations [1, 7–17], speed of read and write operations [5], and transient error rate in an SRAM block [18–20]. Other techniques include implanting non-operational SRAM cells to monitor a sample of worst-case aging in an SRAM block [2, 21] and inserting ring-oscillators in an SRAM block as an indicator of the aging state of memory cells [22–24]. The main issues with SRAM aging sensors are low accuracy, inability to determine individual cell's aging state, susceptibility to PV, and analog components that are error-prone in nanoscales.

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This work proposes a health monitoring SRAM sensor which addresses these issues. The proposed sensor assesses the SNM of each SRAM cell by putting operational SRAM cells in a race with some non-operational SRAM cells with predefined SNMs, called sensor cells. Winning or losing the struggle indicates whether the operational SRAM cell is stronger or weaker than the sensor cell, respectively. The other main features of the proposed approach are adjustable precision, sensing range, and robustness against PV. The precision and sensing range of the sensor can be adjusted by changing the number of sensor cells with different SNMs. The robustness of sensors to PV can be engineered by changing the sensor cells' size. In our simulation setup, the sensor can monitor the SNM variations of SRAM cells in the range of 275 mV to 325 mV with the precision of 5 mV and the area overhead of less than 0.29%.

II. Preliminaries and Related Work

By shrinking transistors' dimensions, the stability margin of SRAM cells decreases due to the reduced operating voltage. Furthermore, their stability is affected by aging-induced transistors threshold voltage drift. Thereby, SNM assessment of SRAM cells has become increasingly essential to ensure reliable chip operation [9, 10, 25]. The most conventionally accepted metric for SRAM cell stability is SNM, which is the minimum noise that can flip the stored value in a cell [25]. SNM can be measured in different ways. One technique is to insert two noise sources between the corresponding inputs and outputs of the NOT gates in the SRAM cell. By gradually increasing the value of noise sources, the voltage leading to a bit-flip in the cell is measured as the SNM of the SRAM cell.

In another simulation-based technique, SNM is defined by the side length of the smaller square from two largest squares that can be fit inside Voltage Transfer Characteristic (VTC) curve of the SRAM cell. As Fig. 1 demonstrates, the VTC curve of a fresh SRAM cell is symmetrical, and thus the highest SNM is achievable. This value is about 267 mV in our configuration. By symmetrical threshold voltage change of the SRAM transistors by 15%, for example due to aging or PV, the SNM decreases to 218 mV, which is observed as VTC curve shrinkage. However, the asymmetric threshold voltage change of the SRAM cell transistors could drastically decrease the cell SNM to about 196 mV. In this condition, the SNM is different when holding '0' or '1'.

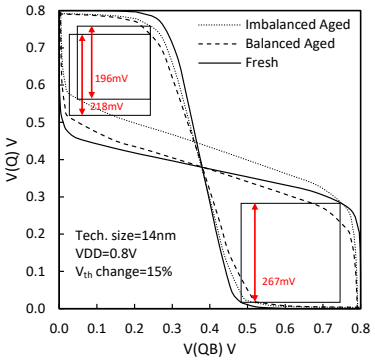

Fig. 1. Aging effect on SNM degradation of the SRAM cell

The SNM can be measured during hold or read operations, and generally, read-SNM is smaller than hold-SNM. This is due to the shunting effect of SRAM access transistors that imposes a glitch on the internal node of the SRAM cell, holding the low-level state. The SNM can also be measured when SRAM cell contains '0' (SNM-zero) or '1' (SNM-one).

The minimum SNM of the cells in an SRAM block determines the minimum possible operating voltage (VDD_{min}), at which the memory block still guarantees the required reliably level. By monitoring the SNM degradation of SRAM cells, a system can take advantage of different techniques to manage power and mitigate aging. Moreover, monitoring ensures a reliability level for the SRAM cells. However, SNM assessment in a fabricated chip is more challenging than in simulation. The reason is that an SRAM cell with a degraded SNM level may still operate correctly under field operation conditions while it is susceptible to environmental noise and prone to faults. Furthermore, the large size and high density of SRAM blocks make the aging assessment more knotty compared to combinational units [26]. The aging sensors for SRAMs can be categorized into five categories:

Current Monitoring Sensors monitor the current drawn by an SRAM memory block from the power rail, during hold [1, 9, 10] or write [11, 12] operations. The deviation in the current consumption during these operations is translated into the aging/robustness condition of the SRAM block. The accuracy of this type of sensors is low, and they only could measure the aging/robustness of an entire SRAM block, and not an individual cell. In another group in this category, the sensor monitors the current of each bitline during a semi-write test condition [7, 8, 13–17]. In general, the accuracy of current monitoring techniques for SNM assessment is highly disputable. This is because in nano-scale fabrication technologies, analog components, as the main parts of these sensors, are more sensitive to noise and PV.

Read/Write Speed Sensors monitor the read/write operations speed as an indicator for aging [5]. This type of sensors can monitor the aging condition of each cell in an SRAM memory block. However, the aging effect on SRAM transistors are not the same, and in some cases, aging may even increase the write speed by lowering the cells' write margin. Furthermore, this type of sensors does not assess the SNM, which is highly affected by aging.

Error-Rate Monitoring Aging Sensors use the built-in Error Correcting Code (ECC) unit to monitor the aging of SRAM cells [18–20]. The error detection/correction rate is a gauge to determine the average aging state of SRAM cells. Another SRAM aging meter is the read-disturbance fault rate, measured by over-driving the wordlines [27].

Sample Monitoring Technique monitors aging of some non-operational SRAM cells [2] or the threshold voltage shift of sample transistors [21] inserted in the SRAM block. Based on this, the overall aging condition of the memory block can be estimated. However, the estimation is based on the worst-case scenario rather than the real aging condition of operational cells. Furthermore, PV can remarkably reduce the accuracy of aging estimation in this type of sensor.

Ring-Oscillator-Based Aging Sensors use the SRAM cells as an active load in an oscillator [22–24]. The oscillation frequency changes by the saturation drive current of under-test SRAM cell transistors. While the digital output is advantageous to this type of sensor, translating the sensor output frequency to SNM is a challenge and the parasitic capacitance of bitlines can affect aging assessment accuracy.

III. The Proposed Aging Sensor

All of the previously proposed techniques to assess SRAM aging are predictive, meaning that they monitor some parameters, and then translate them to an aging level of SRAM cells. Unlike these techniques, our proposed aging sensor could directly determine the SNM of SRAM cells, which is the most vulnerable parameter to memory cells' aging. The proposed sensor operates based on the comparison of cells' SNM and some gauges. This technique puts each operational SRAM cell in a race with some non-operational SRAM cells with predefined SNMs. This approach could determine the SNM level of each SRAM cell in a memory block.

A. Proposed Sensor Functionality

Fig. 2 shows the connection of one sensor cell to an under-test SRAM cell. The sensor cell structure is identical to the operational SRAM cells in a memory block, except the SNM of the sensor which may differ. For aging assessment, the stored value in the operational cell should differ from the stored value in the aging sensor. As shown in the example of Fig. 2, the under-test SRAM cell and the sensor cell store '0' and '1', respectively. When the *wordline (WL)* and *Sensor Select* are activated simultaneously, the current flow through *T1* and *M3* and also through *M2* and *T4*. This makes a race condition between the sensor cell and the SRAM cell to control bitlines (*BL* and *BLB*). Finally, the stronger one overpowers the other in this struggle, and as a result, the stored value in the looser cell flips. If the operational SRAM cell is the winner of the struggle, it means its SNM is higher than that of the sensor, and vice versa. This base structure can assess the SNM of each SRAM cell in a memory block.

To eliminate the effect of bitlines parasitic capacitance on the test result, bitlines are precharged to VDD, similar to the read phase. By doing this, the under-test SRAM cell tries to discharge one bitline, and at the same time, the sensor cell tries to discharge the other bitline. Both cells also try to preserve the charge of the opposite bitline. Thus, the same initial condition, for the sensor cell and the under-test SRAM cell, minimizes the bitlines parasitic capacitance effect on

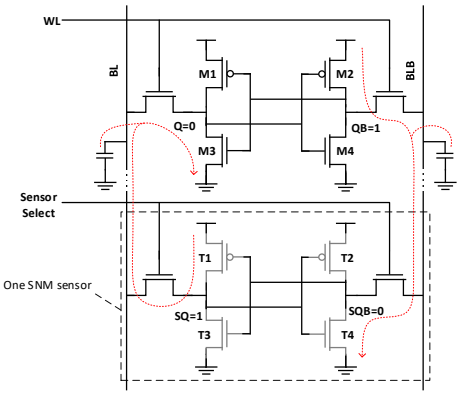

Fig. 2. One sensor cell connected to an operational SRAM cell

the assessment process. Furthermore, regarding the demand for read-SNM or hold-SNM assessment, by predefining the read-SNM or write-SNM of the sensor, each or both of these parameters can be assessed.

To assess the SNM of the under-test SRAM cell with higher precision, several sensor cells with different predefined SNMs can be considered in the design. The under-test SRAM cell is put in the struggle with each of the sensor cells from the weakest to the strongest. The SNM of the under-test SRAM cell is between the SNM of the sensor cells in which the bit flip happens. The desirable precision of the sensor can be obtained by increasing the number of sensor cells.

To prevent the sensor cell from aging, its power is gated during normal system operation. Therefore, the sensor is inactive most of the time and is robust against aging [7]. The slight effect of power-gating transistors' IR drop on sensor SNM can be considered during design time for a more accurate sensor. There are different techniques to adjust the SNM of sensor cells. The sensor transistors' length can be modified while keeping the transistors' width constant. Among the other techniques are changing transistors threshold voltage by body biasing or changing the oxide thickness and channel dopants.

Both of the SNM-zero or SNM-one of SRAM cells can be assessed by the proposed sensor. This is possible by changing the initial stored value in the operational cell as well as the sensor cells. It is worth mentioning that due to imbalanced signal probability on SRAM cells, and consequently imbalanced aging, in many cases the SNM-zero and SNM-one of an aged SRAM cells may differ considerably.

B. Mounting the Proposed Sensor in a Memory Block

To minimize a memory access delay and an area overhead of peripherals in an SRAM memory block, each memory block consists of one or more memory arrays, arranged in $M \times N$ matrix of cells. Generally, M and N are close to each other (both 256 or 512) to maximize memory size while keeping bitlines and wordlines parasitic capacitance low. For memory access, a wordline is activated by the row decoder, and then a column decoder selects K bits from the activated bitlines. The number of accessed bits during each SRAM memory array access is determined by K, which is usually between 1 to 64.

Different configurations of sense amplifiers and write circuits can be considered for SRAM memory arrays. In the architecture shown in Fig. 3, the sense amplifiers are located after the column decoder. In this case, each sense amplifier

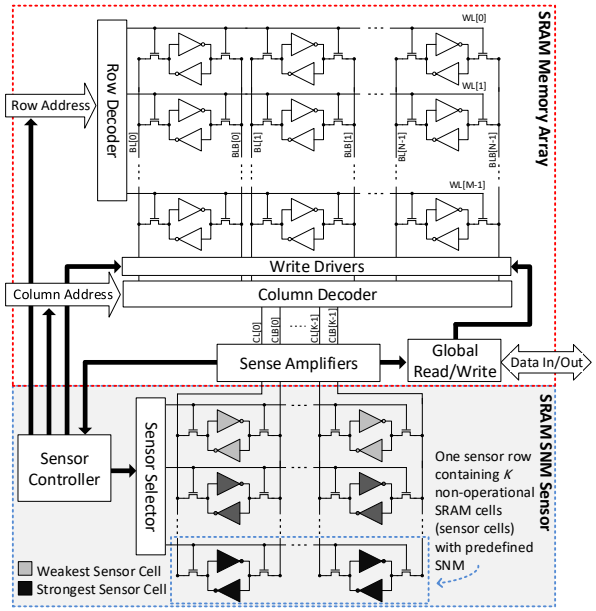

Fig. 3. SRAM sensors located in the memory block

can be shared among the multiplexed columns, and thus, the area overhead of sense amplifiers could be reduced. The write drivers can be located after the column decoder as well. However, to increase the write speed, the write drivers can be directly connected to the bitlines. Generally, the column decoder is made by pass transistors to pass the tiny voltage change on bitlines during a read operation.

Fig. 3 demonstrates the connection of the proposed SRAM sensor to a memory array. Reusing the SRAM memory array peripherals for sensing operation minimizes the sensor controller unit area and complexity. The sensor cells are organized from the weakest to the strongest in a column, while each row consists of K cells. The aging assessment process destroys the data stored in the SRAM memory block. Thus, the aging assessment should be performed during reboots or when no valuable data is stored in the SRAM memory block.

Algorithm 1 presents the SNM assessment procedure of an SRAM array. At the beginning of the test, all operational SRAM cells are filled with '0' to determine SNM-zero. Similarly, they can be set to '1' to determine SNM-one. This setting can be simply performed by filling the write driver with '0' or '1' by the *Sensor Controller* and using a $\log_2^M$-bit counter, where M is the number of SRAM rows, to generate row address (line 1-2).

The SNM assessment is performed for K cells in each assessment round, i.e., equal to the number of sensor cells in each sensor row. Based on this, the aging assessment procedure is repeated from row 0 to row $M-1$. The assessment is then performed $\frac{N}{K}$ times for each SRAM row, where N is the number of cells in the SRAM row (line 3-4).

The opposite of the stored value in SRAM cells is written into all sensor cells (line 5). This can be performed by the SRAM array write drivers. The write drivers are first filled with the required value, and then the column decoder is activated. Finally, the j^{th} chunk of K bitline pairs are connected to the columns through the column decoder (line 6).

Upon starting the race, bitlines, column decoder, and

Algorithm 1: Flow of SRAM array SNM assessment

```
1  all of operational SRAM cells ← 0/1;
2  power On sensor;
3  for i=0; i< M; i++ do
4      for j=0; j< N/K; j++ do
5          all of sensor cells ← 1/0;
6          column address ← j;
7          for s=0; s<number of sensor rows; j++ do
8              precharge bitlines and columns to VDD;
9              simultaneously: WL(i) ← 1,
10             Sensor Select(s) ← 1;
11             wait for stabilization of cells and sensors in the race;
12             read the stabilized value in selected columns;
13             if any of SRAM cells is flipped in this round then
14                 the SNM of flipped cells at this round is in the
                       range of Sensor Row(s) and Sensor Row(s-1);
15             if all of the selected SRAM cells are flipped then
16                 break;
17 power Off sensor;
```

columns are precharged to *VDD* (line 8). Then, the sensor cells, from the weakest to the strongest, are put in the race with the selected operational SRAM cells. The required time to decide the race's winner ($T_{stabilize}$) is mainly determined by the parasitic capacitance of bitlines, i.e., comparable to the write operation time in the memory array. After this period of time, the selected columns are read by activating the sense amplifiers. If the stored values in the selected SRAM cells do not flip, it means the SNM of the selected SRAM cells is higher than the selected sensor row. Thereby, the bitlines, column decoder, and columns are precharged to VDD, and the procedure is repeated by selecting the next stronger sensor row (from line 7). If any of the stored values is flipped, it indicates the SNM of the selected cells is between the SNM of the sensor row and the SNM of the previous sensor row (line 13-14). An SNM assessment round finishes if all selected SRAM cells are flipped, or the strongest row of the sensor was selected (line 15-17). If determining the worst-case of SNM (the lowest SNM) in the selected SRAM cells is the demand (which is, in many cases), the test of each selected SRAM cells chunk is ended after determining the first bit-flip.

For each sensor row, the number of SNM assessment rounds is equal to $\frac{M \times N}{K}$. Thereby, the total assessment time depends on the number of sensor rows and $T_{stabilize}$ as well as the aging state of the selected SRAM cells. Since the SRAM aging status is assessed in long time intervals, the aging assessment time, which is in the order of microseconds, is not a notable concern, but still part of our future work.

In sum, the main outstanding advantages of the proposed SNM sensor are as follows:

- The result of each aging assessment round is automatically stored in the under-test SRAM cells within the block. The result can be used for power management or reliability improvement decisions. This benefit eliminates the need for extra memory space to store the aging pattern of the SRAM memory block.
- The proposed sensor does not contain analog parts, and thus the sensor accuracy is enhanced in nanoscale technology sizes.
- Area overhead is negligible in comparison with the memory block size.
- The sensor is robust against temperature as SRAM and sensor cells enjoy the same structure in which the temperature effect is differentially canceled out.
- The sensor is capable of assessing the aging status of individual cells in an SRAM block.

C. Sensor Accuracy in the Presence of PV

The primary and most uncontrollable source of PV in nanoscale technology sizes is Random Dopant Fluctuation (RDF) [9, 10], which occurs due to variations in the implanted impurity concentration. The other serious PV sources are the change in the channel size and shape, and oxide thickness, which have increased in the nanoscale technology sizes.

The analytical expression for the V_{th} standard deviation (σ) shows that the key features for the PV control are oxide thickness, effective length (L_{eff}) and width (W_{eff}), and doping concentration of transistors. Between these features, L_{eff} and W_{eff} are more flexible to be adjusted, and thus, in this work, width and length enlargement is applied to make the sensor robust against PV [2].

Transistor variability is inversely proportional to the channel area ($W \times L$) [2]. Eq. (1) shows the relation between the variance (σ^2) in V_{th} of transistors as the manifested effect of PV at the circuit-level and the channel area (Ch_{Area}).

$$\sigma^2 \propto \frac{1}{Ch_{Area}} \propto \frac{1}{W \times L} \tag{1}$$

IV. Experimental Evaluation

To evaluate the proposed SRAM aging sensor, $14\,nm$ Multi-Gate technology node is utilized for circuit simulation using HSPICE. The correctness of sensor operation, the effect of bitlines parasitic capacitance, and the robustness of the sensor against PV are evaluated. The SNM of SRAM and sensor cells are modified depending on the transistor threshold voltage change. The simulation parameters are shown in Table. I.

We compare the proposed sensor with the ring-oscillator-based sensor presented in [23]. Among state-of-the-art sensors, this sensor is selected for comparison as it has the closest sensing scheme to the proposed sensor.

The PV effect at the circuit-level can be modeled by the threshold voltage change of transistors. We considered Gaussian distribution for PV modeling, which randomly drifts the threshold voltage of the sensor transistors with the mean of m and standard deviation of σ ($V_{th}(m, \sigma)$). The Monte Carlo simulation method with 500 iterations is considered to extract the PV effect on different sensor sizes.

A. Health Monitoring

Fig. 4 shows the voltage changes of the nodes *Q* and *QB* (see Fig. 2) for the under-test SRAM cell with different SNMs of

TABLE I
Circuit Simulation Parameters

Technology node	14 nm PTM-MG
VDD	0.8 V
SRAM cell (W×L nm^2)	Pull-Up: 14×14, Pull-Down: 35×14, Access: 14×14
PV-Resistant Sensor cell	2x, 3x, 4x, and 5x of SRAM cell
C_{BL}	10 fF ~ 200 fF (144 fF Nominal)

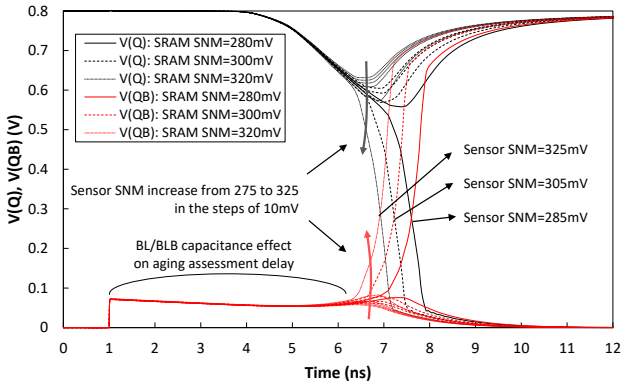

Fig. 4. Health monitoring of under-test SRAM cell

280 mV, 300 mV, and 320 mV. In this case study, we consider six sensors, and the sensors' SNM increases from 275 mV to 325 mV in the steps of 10 mV. The weakest sensor cell (i.e., SNM of 275mV) is first put in the struggle with the under-test SRAM cell. Since the sensor is weaker than the under-test SRAM, the struggle leads to a glitch in the *Q* and *QB* nodes of the SRAM cell. The glitch on the SRAM node which holds '1' (in this case *Q*) is larger than the other node. This value is about 160 mV to 240 mV depending on the bitlines capacitance and the SRAM and sensor strengths. The larger glitch on the node holding '1' is due to stronger pull-down transistors in the SRAM cell.

By increasing the sensor strength in the test process, the sensor may overpower the SRAM cell, determining the SNM range of the SRAM cell. In our evaluation, the sensors with 285 mV, 305 mV, and 325 mV are the sensors which overpower three different under-test SRAM cells. According to the results, the strength of the weakest SRAM cell is detected to be between 275 mV and 285 mV. The strength of the second SRAM cell is between 295 mV and 305 mV. Finally, the strength of the strongest SRAM cell is between 315 mV and 325 mV.

The under-test SRAM cell and the sensor cell are connected to the bitlines at time 1 ns. The *QB* is elevated by 72 mV due to large capacitance of connected bitline (144 fF in this evaluation), which is precharged to VDD. In our configuration, a delay of about 5 ns occurs before the SRAM or sensor flips. This delay is a function of bitlines capacitance. Fig. 5 shows the effect of bitlines capacitance (C_{BL}, C_{BLB}) on the sensor delay. At each phase of aging assessment, *BL* and *BLB* start to discharge to the trigger point (e.g., about 183mV) via pull-down transistors of the SRAM and sensor cells. This value is determined by pull-up, pull-down, and access transistor sizes. Reaching the trigger point, either the SRAM cell or the sensor cell flips its value and fully discharge *BL* or *BLB*. The other bitline does not fully charge to VDD since n-type access transistor drops the output by V_{th}. The increase of bitlines capacitance from 10 fF to 200 fF, which is the function of memory array size, extends $T_{stabilize}$ from 2 ns to about 10 ns. For this evaluation, the weakest sensor, which can flip the SRAM cell, is selected, imposing the longest stabilization delay.

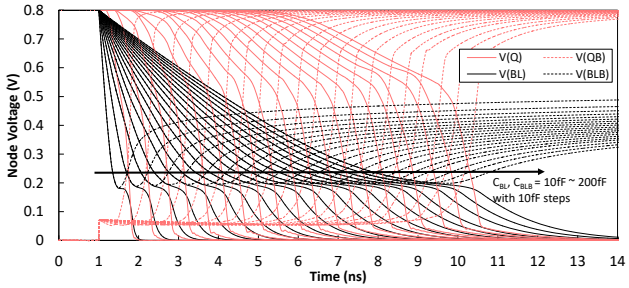

Fig. 5. The effect of bitlines capacitance on sensor stabilization time

B. Process Variation

In this work, the shift in V_{th} is considered as the circuit-level manifestation of PV in transistor parameters. To assess the effect of PV on the sensor accuracy, we utilized Monte Carlo simulation using HSPICE. The Gaussian distribution with the standard deviation (σ) of 15% for V_{th} drift in 14 nm technology node is assumed in this work. By enlarging the sensor cells' transistors, it is expected that the variance in the V_{th} of fabricated transistors decreases with Eq (1). Fig. 6 shows the effect of different sensor cell sizes on sensor SNM fluctuations. When the sensor cell size is the same as the operational SRAM cell, the standard deviation of the sensor cells' SNM is 18.73 mV. By increasing the sensor cell size by 2x, 3x, 4x, and 5x, the standard deviation of SNM decreases by 9.41,mV, 6.33 mV, 4.74 mV, and 3.83 mV, respectively. Thereby, the desired sensor accuracy can be accurately adjusted based on demand and with an acceptable area overhead.

C. Area Overhead

The area overhead of the proposed sensor depends on the required accuracy. Since the number of sensor cells is far less than the SRAM cells for an SRAM array, increasing the sensor cells' size does not impose considerable area overhead. In many cases, only one sensor row (8 sensor cells) suffices to detect the SNM violation of SRAM cells from a predefined threshold. Since sensors can be located after the column decoder in the SRAM block, there is no pitch-matching issue to insert the sensor in the memory block.

To evaluate the area overhead of the proposed sensor, compared with a 64 Kb (256×256) SRAM array, we used Synopsys Design Compiler with NanGate FreePDK 15 nm, closest to the utilized circuit-level model, as an open-source library. The area of the SRAM array is extracted using CACTI 6.5. The counters of SRAM bitlines and wordlines, comparator, and the row selector in the sensor controller, together with the sensor cells, are the largest units in the sensor, which we have implemented them in Verilog.

TABLE II
SENSOR AREA COMPARING WITH A 256×256 CELL SRAM ARRAY

	1x	2x	3x	4x	5x
1-row	0.16 %	0.20 %	0.25 %	0.33 %	0.43 %
2-row	0.18 %	0.24 %	0.35 %	0.51 %	0.71 %
5-row	0.22 %	0.39 %	0.66 %	1.05 %	1.55 %
10-row	0.29 %	0.63 %	1.18 %	1.95 %	2.95 %

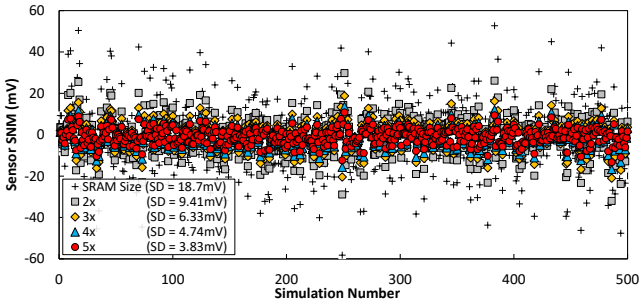

Fig. 6. The effect of sensor size on accuracy at the presence of PV

Table II shows the imposed area overhead of the sensor with 1, 2, 5, and 10 rows, and eight sensor cells in each row. The area overhead of the sensor cells with W and L enlargement of 1x to 5x is also considered for PV mitigation. The 1x sensor size imposes the least area overhead of up to 0.29 % for a 10-row configuration. By increasing the sensor cell size, the area overhead increases by 2.95 % with the precision of 10 levels. By increasing the memory array to 256 Kb, this value decreases by 0.79 %. The area of power-gating transistors is not accounted in the reported areas.

D. Comparison with the Prior Art

We compare the proposed sensor with the ring-oscillator-based sensor presented in [23] in the presence of PV. For this aim, we implemented the ring-oscillator sensor structure with the same technology as our proposed sensor. The standard deviation of assessed SNM of the ring-oscillator sensor in 500 rounds of Monte Carlo simulation is 12.9%, 6.2%, 4.1%, 3.0%, and 2.5% for 1x, 2x, 3x, 4x and 5x sensor sizes, respectively. These values are 7.0%, 3.2%, 2.4%, 1.8%, and 1.4% for the proposed sensor. The higher error rate in the ring-oscillator sensor is due to the non-linear relation between the output frequency and the SNM of the under-test SRAM. Small changes (smaller than 30 mV) in SNM lead to a very slight change in the output frequency of the ring-oscillator sensor, which makes this sensor more sensitive to PV. Furthermore, ring-oscillator sensors are susceptible to temperature change (more than 18% in $100\,^{\circ}C$ [23]) whereas the temperature variations effect on the proposed sensor is almost negligible. This is due to the same effect of temperature on the operational SRAM cells and sensor cells.

For a wider comparison, in Table III, we logically compare the state of the art aging sensors, reviewed in Section II, with the proposed sensor. The comparison is made with regard to area, accuracy, sensitivity to PV, sensitivity to temperature, and the sensing range. This table shows the advantage of the proposed design in different aspects.

V. Conclusion

Aging leads to variation in the SNM of the SRAM cells. Thus, monitoring the stability of SRAM memories is vital to ensure reliable and low power chip operation. Due to the high complexity and size of SRAM structures, monitoring the health condition of each SRAM cell is very challenging and usually relies on analog solutions. This work proposes a comparative technique to assess the SNM of individual SRAM cells in an SRAM memory array with an adjustable precision and robustness level.

TABLE III
Comparison of proposed aging sensor with the previous work

	Area (%)	Accuracy	PV Sensitivity	Temp. Sensitivity	Sensing Range
Current Monitoring [1, 7–17]	<1	low∼medium	very high	very high	high
R/W Speed Monitoring [5]	N/A	medium	low	high	high
Error Rate Monitoring [18–20, 27]	<1	low∼medium	low	medium	low
Sample Monitoring [2]	$<1\sim3.4$	low∼medium	very high	very low	high
Ring-Oscillator-Based Sensor [22–24]	$<0.5\sim1$	high	high	high	high
The proposed sensor	$<0.2\sim2.9$	low∼very high	low	very low	high

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