Virtual memory - Paging

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The process

Memory layout for a 32-bit Linux process
Segments - a could be solution

Processes in virtual space

Address translation by MMU
(base and bounds)

Physical memory
Segments - a could be solution

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Processes in virtual space

Address translation by MMU (base and bounds)

Physical memory
one problem

Physical memory
External fragmentation: free areas of free space that is hard to utilize.
External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ...
External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ... internal fragmentation.
another problem

virtual space

physical memory
another problem

virtual space

physical memory
another problem

virtual space

code

physical memory
another problem

virtual space  

physical memory

code
another problem

virtual space

used  code

physical memory
another problem

virtual space

used

code

physical memory

not used?
We’re reserving physical memory that is not used.
Let’s try again
Let’s try again

It’s easier to handle fixed size memory blocks.
Let’s try again

It’s easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?
Let’s try again

It’s easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?

An address is interpreted as a virtual page number (VPN) and an offset.
Remember the segmented MMU

virtual addr. + offset → within bounds

index → segment table

physical address

exception → no

yes
The paging MMU

MMU

virtual addr.
The paging MMU

MMU

virtual addr.
The paging MMU

MMU

virtual addr.  

/ /

page table
The paging MMU

MMU

virtual addr.

VPN

page table
The paging MMU

MMU

virtual addr.  offset

VPN

page table
The paging MMU

MMU

virtual addr. + offset = physical address

VPN → page table
The paging MMU

MMU

virtual addr. \[ \text{VPN} \]

offset

page table

physical address

\[ \text{VPN} + \text{offset} \rightarrow \text{physical address} \]
The paging MMU

MMU

virtual addr. // offset

VPN

page table

exception

available

physical address
the MMU

virtual address

Segmentation
the MMU

virtual address

Segmentation

linear address
the MMU

Segmentation

virtual address → within bounds → linear address

exception
virtual address → exception

within bounds

Segmentation

linear address → Paging
the MMU

virtual address → exception
           ↓
within bounds
Segmentation
linear address → Paging
the MMU

virtual address → exception
    within bounds
    Segmentation
    linear address → physically available

Paging
    physical address
The x86-32 architecture supports both segmentation and paging. A virtual address is translated to a *linear address* using a segmentation table. The linear address is then translated to a physical address by paging.
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Still used to manage *thread local storage* and *CPU specific data*. 
Processes in virtual space

Physical memory
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Only pages actually used need to be in memory.
virtual space

physical memory
virtual space

physical memory
virtual space

physical memory
virtual space

available

physical memory
three pages

virtual space

available
not available (page fault)
not allocated (segmentation fault)

physical memory
The pagetable

The MMU page module

The page table provides translation from page numbers to frame numbers, kernel or user space read and write access rights available in memory or on disk.

Note: the page table is too large to fit into the MMU hardware, it is in main memory.
The pagetable

The MMU page module

The page table
- provides translation from page numbers to frame numbers
- kernel or user space
- read and write access rights
- available in memory or on disk
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The page table entry

example Linux on (32bit) x86

31
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If the page index is 20 bits, does the frame number need to be 20 bits?
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In 1995 the x86 architecture provided 24-bit frame numbers. The CPU could thus address 64 Gibyte of physical address space (24-bit frame, 12-bit offset). Each process still had a 32-bit virtual address space, (20-bit page number, 12-bit offset) i.e. 4 Gibyte.

The x86_64 architecture supports 48-bit virtual address space and up to 52-bit physical address space.

Linux supports 48-bit virtual address (47-bit user space) and up to 46-bit physical address space (64 Tibyte). Check your address space in /proc/cpuinfo.

Physical memory is in reality limited by chipset, motherboard, memory modules etc. Check your available memory in /proc/meminfo.
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Largest server on the market, SGI 3000, can scale up to 256 CPUs and 64 Tbyte of RAM (NUMA) - running Linux.
Speed matters

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we need a page table base register, PTBR

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An extra memory operation for each memory reference.

17 / 32
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Who handles a TLB miss

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- MIPS, Sparc, ARM
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What happens when we switch process?
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virtual addr.
The paging MMU with TLB

virtual addr.
The paging MMU with TLB

virtual addr.  

/\  

VPN  

TLB
The paging MMU with TLB

virtual addr. \[\rightarrow\] VPN \[\rightarrow\] offset \[\rightarrow\] TLB \[\rightarrow\] PFN \[\rightarrow\] physical address
The paging MMU with TLB

virtual addr. → VPN → TLB → PFN → offset → physical address

VPN

PFN

PTBR
The paging MMU with TLB

virtual addr. → offset → VPN → TLB →PFN ↑ → + → physical address

VPN → PTBR → + → VPN
The paging MMU with TLB

virtual addr. → offset → VPN → TLB → PFN → PTBR → VPN → physical address

Page table in memory
The paging MMU with TLB

virtual addr.  \rightarrow  offset

\rightarrow  VPN

\rightarrow  TLB

\rightarrow  PFN

\rightarrow  physical address

\rightarrow  VPN

\rightarrow  PTE

\rightarrow  PTBR

\rightarrow  Page table in memory
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Problem!
Why not use pages of size 4 Mibyte?
The solution - not.

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4 Mibyte pages are used and do have advantages but it is not a general solution.
Mostly empty space

- code (.text)
- data
- heap
- stack
- kernel

Map only the areas that are actually used.
Mostly empty space

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What if each segment was rarely larger than 1Ki pages of 4Kibyte.
Hybrid approach - paged segmented memory

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Hybrid approach - paged segmented memory

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- **bound**: base/bound
- **base**: page table
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Multi-level page table

Used by Intel 80386
Multi-level page table

31  22  0

10-bit directory index

*Used by Intel 80386*
### Multi-level page table

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page directory

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- **Page directory**
- **Page table**

*Used by Intel 80386*
Multi-level page table

![Diagram of multi-level page table]

- 10-bit directory index
- 10-bit page index
- 12-bit offset

Used by Intel 80386
Multi-level page table

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Used by Intel 80386
Multi-level page table

Used by Intel 80386
Mostly empty space

page directory

virtual address space
Mostly empty space

page directory

virtual address space
Mostly empty space

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Mostly empty space

page directory

virtual address space
Mostly empty space

page directory

each page table can map 4 Mibyte

virtual address space
More than two levels

Scheme used in PAE, where each entry has a 24-bit physical base address. Each page table entry was 8 bytes wide.

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
More than two levels

2-bit page global directory index
More than two levels

- 2-bit page global directory index
- 9-bit page middle directory index

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
More than two levels

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9-bit page middle directory index

9-bit page table index

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- 9-bit page middle directory index
- 9-bit page table index
- 2-bit page global directory index
- 12-bit offset

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- 9-bit page upper directory index
- 9-bit page lower directory index
- 9-bit page table index
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A page table entry is 8 bytes and contains a 40-bit physical address base address.
The x86_64 architectures

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Linux can only handle a physical base address of 34 bits i.e. 46 bit physical address.
Inverted page tables

Why not do something completely different?

We will probably not have more than say 8 Gibyte of main memory.

If we divide this into 4 Kibyte frames we have 2 Mi frames.

Assume maintain a table with 2 Mi entries that describes which process and page that occupies the frame.

To translating a virtual address we simply search the table (efficient if we use a hash table).

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Speed of translation is a problem (what is the solution?)
The size of the page table is a problem (and you know how to solve it).
Inverted page tables - an alternative approach.
TLB - dynamite, makes paging possible.