Virtual memory - Paging

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KTH

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Memory layout for a 32-bit Linux process
Segments - a could be solution

Processes in virtual space

Address translation by MMU
(base and bounds)

Physical memory
Segments - a could be solution

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Physical memory

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Physical memory
Segments - a could be solution

Processes in virtual space

Address translation by MMU (base and bounds)

Physical memory
External fragmentation: free areas of free space that is hard to utilize. Solution: allocate larger segments to reduce internal fragmentation.

Physical memory
External fragmentation: free areas of free space that is hard to utilize.
External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ...
External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ... internal fragmentation.
another problem

---

virtual space

---

physical memory
another problem

---

code

---

virtual space

---

physical memory
another problem

virtual space

physical memory
another problem

virtual space

physical memory
another problem
another problem

virtual space

physical memory
We’re reserving physical memory that is not used.
Let’s try again

It’s easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?

An address is interpreted as a virtual page number (VPN) and an offset.
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It’s easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?

An address is interpreted as a *virtual page number* (VPN) and an *offset*. 
Remember the segmented MMU

MMU

virtual addr. → offset → < → yes → within bounds

index → segment table → + → physical address

exception → no
The paging MMU

MMU

virtual addr.

The paging MMU

MMU

virtual addr.  //

page table
The paging MMU

MMU

virtual addr.

VPN

page table
The paging MMU

MMU

virtual addr. + offset

VPN

page table
The paging MMU

MMU

virtual addr. //

page table

VPN

offset

+ 

physical address

8 / 31
The paging MMU

MMU

virtual addr.  offset

VPN

-page table

physical address
The paging MMU

virtual addr. // offset

VPN

page table

exception

available

physical address
the MMU

virtual address

Segmentation
the MMU

virtual address

Segmentation

linear address
the MMU

virtual address → exception

within bounds

Segmentation

linear address
the MMU

virtual address → exception

within bounds → Paging

Segmentation

linear address
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virtual address → exception → within bounds → Paging

Segmentation

linear address
the MMU

virtual address → exception → within bounds → Paging

Segmentation → linear address → physical address
the MMU

- Virtual address
- Exception
- Within bounds
- Segmentation
- Linear address
- Paging
- Page available
- Physical address
The x86-32 architecture supports both segmentation and paging. A virtual address is translated to a *linear address* using a segmentation table. The linear address is then translated to a physical address by paging.
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Still used to manage *thread local storage* and *CPU specific data*. 
the process

Processes in virtual space

Physical memory
Processes in virtual space

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Processes in virtual space

Only pages actually used need to be in memory.

Physical memory
virtual space

physical memory
virtual space

physical memory
virtual space

physical memory
virtual space

available

physical memory
virtual space

available

not available (page fault)

physical memory
virtual space

available

not available (page fault)

not allocated (segmentation fault)

physical memory
example Linux on (32bit) x86
example Linux on (32bit) x86
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If the page index is 20 bits, does the frame number need to be 20 bits?
example Linux on (32bit) x86

The page table entry

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The x86_64 architecture supports 48-bit virtual address space and up to 52-bit physical address space.

Linux supports 48-bit virtual address (47-bit user space) and up to 46-bit physical address space (64 TiB). Check your address space in `/proc/cpuinfo`.

Physical memory is in reality limited by chipset, motherboard, memory modules etc. Check your available memory in `/proc/meminfo`. 
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Physical Address Extension (PAE)

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Physical memory is in reality limited by chipset, motherboard, memory modules etc. Check your available memory in `/proc/meminfo`. 
Largest server on the market, SGI 3000, can scale up to 256 CPUs and 64 Tbyte of RAM (NUMA) - running Linux.
we need a page table base register, PTBR

movl 0x11111222, %eax
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Speed matters

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Who handles a TLB miss

**RISC architecture**
- MIPS, Sparc, ARM
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- The hardware raises an interrupt.
Who handles a TLB miss

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- The hardware will access the page table and updates the TLB.
What happens when we switch process?

The TLB contains the cached translations of the running process, when switching process the TLB must (in general) be flushed. Do we have to flush the whole TLB? Is this best handled by the hardware or operating system? Can we do pre-fetching of page table entries?
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Can we do pre-fetching of page table entries?
virtual
daddr.
The paging MMU with TLB

virtual addr. //
The paging MMU with TLB

virtual addr.
The paging MMU with TLB

virtual addr. -> TLB

VPN
The paging MMU with TLB

virtual addr. → VPN → offset → TLB → PFN → + → physical address
The paging MMU with TLB

virtual addr. → offset

VPN → TLB → PFN + → physical address

PTBR
The paging MMU with TLB

virtual addr. -> offset

VPN -> TLB

VPN -> PTBR

PFN + -> physical address

PFN + -> PTBR
The paging MMU with TLB

virtual addr. → offset → VPN

VPN → TLB → PFN

PFN + PTBR → physical address

Page table in memory
The paging MMU with TLB

- Virtual address
- Offset
- VPN
- TLB
-PFN
- Physical address
- PTE
- PTBR
- Page table in memory
Using 4 Kbyte pages (12 bits) for a 4 Gibyte address space (32 bits) will result in 1Mi (20 bits) page table entries.
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Each process has its own page table.
Size matters

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For 100 processes we need room for 400 Mibyte of page tables.
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Problem!
Why not use pages of size 4 Mibyte?
The solution - not.

Why not use pages of size 4 Mibyte?

- Use a 22 bit offset and 10 bit virtual page number.
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- Case closed!
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4 Mibyte pages are used and do have advantages but it is not a general solution.
Map only the areas that are actually used.
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Map only the areas that are actually used.
What if each segment was rarely larger than 1Ki pages of 4Kibyte.
Hybrid approach - paged segmented memory

What if each segment was rarely larger than 1Ki pages of 4Kibyte.

<table>
<thead>
<tr>
<th>seg</th>
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<tbody>
<tr>
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<td>29</td>
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What if each segment was rarely larger than 1Ki pages of 4Kibyte.

| seg | 18-bit page number |
Hybrid approach - paged segmented memory

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base/bound
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Diagram:
- Seg: Base/Bound
- 18-bit page number
- 12-bit offset
- Bound
- Frame number
- Page table
- Base
Hybrid approach - paged segmented memory

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- **seg**: 31 29
- **18-bit page number**: 12
- **12-bit offset**: 0

- **base/bound**
- **bound**
- **page table**
- **frame number**
- **base**
- **page**
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Hybrid approach - paged segmented memory
Multi-level page table

Used by Intel 80386
Multi-level page table

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**Page directory**

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Used by Intel 80386
Multi-level page table

31
10-bit directory index

22
10-bit page index

12
12-bit offset

0

page directory

page table

Used by Intel 80386
Multi-level page table

Used by Intel 80386
Multi-level page table

10-bit directory index | 10-bit page index | 12-bit offset

page directory

page table

page

Used by Intel 80386
Mostly empty space

page directory

virtual address space
Mostly empty space

page directory

virtual address space
Mostly empty space

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page directory

each page table can map 4 Mibyte

virtual address space
More than two levels

Scheme used in PAE, where each entry has a 24-bit physical base address. Each page table entry was 8 bytes wide.

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
More than two levels

2-bit page global directory index
More than two levels

31 29 21 0

9-bit page middle directory index

2-bit page global directory index

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More than two levels

9-bit page table index

9-bit page middle directory index

2-bit page global directory index

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More than two levels

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The x86_64 architectures

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- Bits 63-47 are either 1, kernel space, or 0, user space.
- The 48 bits are divided into:
  - 9-bit page global directory index
  - 9-bit page upper directory index
  - 9-bit page lower directory index
  - 9-bit page table index
  - 12-bit offset
- A page table entry is 8 bytes and contains a 40-bit physical address base address.
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- A page table entry is 8 bytes and contains a 40-bit physical address base address.
- The 40-bit base is combined with the 12-bit index to a 52-bit physical address.
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*Linux can only handle a physical base address of 34 bits i.e. 46 bit physical address.*
Inverted page tables

Why not do something completely different?

We will probably not have more than say 8 Gibyte of main memory.

If we divide this into 4 Kibyte frames we have 2 Mi frames.

Assume maintain a table with 2 Mi entries that describes which process and page that occupies the frame.

To translating a virtual address we simply search the table (efficient if we use a hash table).

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- Speed of translation is a problem (what is the solution?)
- The size of the page table is a problem (and you know how to solve it).
- Inverted page tables - an alternative approach.
TLB - dynamite, makes paging possible.