Virtual memory - Paging

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KTH

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The process

Memory layout for a 32-bit Linux process
Segments - a could be solution

Processes in virtual space

Address translation by MMU (base and bounds)

Physical memory
Segments - a could be solution

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Processes in virtual space

Address translation by MMU (base and bounds)

Physical memory
one problem

Physical memory

External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments...
one problem

External fragmentation: free areas of free space that is hard to utilize.
one problem

External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ...
External fragmentation: free areas of free space that is hard to utilize.

Solution: allocate larger segments ... internal fragmentation.
another problem

virtual space

physical memory
virtual space

code

physical memory
another problem

virtual space

physical memory
another problem

virtual space

code

physical memory
another problem

virtual space

physical memory

used
code
another problem

virtual space
used

physical memory
not used?
We’re reserving physical memory that is not used.
Let’s try again

It’s easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?

An address is interpreted as a virtual page number (VPN) and an offset.
Let’s try again

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Can we map a process virtual space to a set of equal size blocks?
Let's try again

It's easier to handle fixed size memory blocks.

Can we map a process virtual space to a set of equal size blocks?

An address is interpreted as a *virtual page number* (VPN) and an *offset*. 
Remember the segmented MMU

MMU

virtual addr. → offset → < → yes → within bounds

index → segment table → physical address

exception → no
virtual addr.
The paging MMU

MMU

virtual addr.
The paging MMU

MMU

virtual addr. //

page table
The paging MMU

MMU

virtual addr. → VPN → page table
The paging MMU

MMU

virtual addr.  offset

VPN

page table
The paging MMU

MMU

virtual addr.  offset

VPN

physical address

page table
The paging MMU

MMU

virtual addr. → offset

VPN → page table → ? → physical address
The paging MMU

MMU

virtual addr. \(\rightarrow\) offset

VPN

\[\text{VPN} \rightarrow \text{page table} \rightarrow ? \rightarrow \text{physical address} \rightarrow \text{available} \rightarrow \text{exception}\]
virtual address

Segmentation
the MMU

Segmentation

virtual address → linear address
the MMU

virtual address \rightarrow \text{within bounds} \rightarrow \text{Segmentation} \rightarrow \text{linear address} \rightarrow \text{exception}
the MMU

virtual address ➔ exception ➔ within bounds ➔ Segmentation ➔ linear address ➔ Paging
the MMU

Virtual address → within bounds → linear address → exception → Paging

Segmentation
the MMU

virtual address → within bounds → linear address

Segmentation

exception

Paging

physical address
the MMU

virtual address

Segmentation

within bounds

linear address

Paging

page available

physical address

exception

exception
The x86-32 architecture supports both segmentation and paging. A virtual address is translated to a *linear address* using a segmentation table. The linear address is then translated to a physical address by paging.
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Still used to manage *thread local storage* and *CPU specific data*.
Processes in virtual space

Physical memory
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Physical memory
Processes in virtual space
Processes in virtual space

Only pages actually used need to be in memory.
virtual space

physical memory
virtual space

physical memory
virtual space

physical memory
virtual space

available

physical memory
three pages

virtual space

available

not available (page fault)

physical memory
virtual space

available

not available (page fault)

not allocated (segmentation fault)

physical memory
The page table

<table>
<thead>
<tr>
<th>page number</th>
<th>offset</th>
</tr>
</thead>
</table>

page table
The page table
The page table

- page number
- offset
- frame number

page table
The page table

- page number
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- frame number

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- frame number
- page table
The page table

- page number
- offset
- frame number

page table
The page table
example Linux on (32bit) x86

Valid

31

1
example Linux on (32bit) x86

31  12

20-bit frame number

<table>
<thead>
<tr>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
</tbody>
</table>
The page table entry

example Linux on (32bit) x86

31 12

20-bit frame number

Valid

R/W

If the page index is 20 bits, does the frame number need to be 20 bits?
example Linux on (32bit) x86

The page table entry

31

31

20-bit frame number

12

User/Supervisor

Valid

R/W

1
The page table entry

example Linux on (32bit) x86

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In 1995 the x86 architecture provided 24-bit frame numbers. The CPU could thus address 64 GiB of physical address space (24-bit frame, 12-bit offset). Each process still had a 32-bit virtual address space, (20-bit page number, 12-bit offset) i.e. 4 GiB.

The x86_64 architecture supports 48-bit virtual address space and up to 52-bit physical address space.

Linux supports 48-bit virtual address (47-bit user space) and up to 46-bit physical address space (64 TiB). Check your address space in /proc/cpuinfo.

Physical memory is in reality limited by chipset, motherboard, memory modules etc. Check your available memory in /proc/meminfo.
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Largest server on the market, SGI 3000, can scale up to 256 CPUs and 64 Tbyte of RAM (NUMA) - running Linux.
we need a page table base register, PTBR

movl 0x11111222, %eax
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*An extra memory operation for each memory reference.*
The CPU keeps a *translation look-aside buffer*, TLB, with the most recent page table entries.
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Who handles a TLB miss

**RISC architecture**
- MIPS, Sparc, ARM

The hardware raises an interrupt.
The operating system jumps to a trap handler.
The operating system will access the TLB and update the TLB.

**CISC architecture**
- x86
  - The hardware "knows" where to find the page table (CR3 register).
  - The hardware will access the page table and updates the TLB.
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Which TLB entry should we remove if the TLB is full?
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- 31
- 12
- 20-bit frame number
- Valid
- 1
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31

20-bit frame number

12

Valid

R/W

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Process switching

What happens when we switch process?

The TLB contains the cached translations of the running process, when switching process the TLB must (in general) be flushed. Do we have to flush the whole TLB? Is this best handled by the hardware or operating system? Can we do pre-fetching of page table entries?
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Can we do pre-fetching of page table entries?
The paging MMU with TLB

linear addr.
The paging MMU with TLB

linear addr. //
The paging MMU with TLB

linear addr.
The paging MMU with TLB

linear addr.

/ /

VPN

TLB
The paging MMU with TLB

 linear addr. ------- offset ------- physical address

 VPN -> TLB -> PFN

 offset +
The paging MMU with TLB

linear addr. \rightarrow VPN \rightarrow TLB \rightarrow PFN \rightarrow physical address

offset

PTBR
The paging MMU with TLB

linear addr.  offset

VPN  //  VPN

TLB  PFN

PTBR

physical address
The paging MMU with TLB

linear addr. → offset

VPN → TLB → PFN + → physical address

VPN → PTBR → +

Page table in memory
The paging MMU with TLB

- Linear address
- Offset
- VPN
- TLB
-PFN
- Physical address
- PTE
- PTBR
- Page table in memory
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For 100 processes we need room for 400 Mibyte of page tables.
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Problem!
Why not use pages of size 4 Mibyte?
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- Use a 22 bit offset and 10 bit virtual page number.
The solution - not.

Why not use pages of size 4 Mibyte?

- Use a 22 bit offset and 10 bit virtual page number.
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- Case closed!
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*4 Mibyte pages are used and do have advantages but it is not a general solution.*
Map only the areas that are actually used.
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Hybrid approach - paged segmented memory

What if each segment was rarely larger than 1Ki pages of 4Kibyte.
Hybrid approach - paged segmented memory

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| seg | 31 | 29 | 0 |
Hybrid approach - paged segmented memory

What if each segment was rarely larger than 1Ki pages of 4Ki byte.

<table>
<thead>
<tr>
<th></th>
<th>18-bit page number</th>
</tr>
</thead>
<tbody>
<tr>
<td>seg</td>
<td></td>
</tr>
<tr>
<td>31  29</td>
<td>12 0</td>
</tr>
</tbody>
</table>
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</tr>
<tr>
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<table>
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base/bound
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- **seg**
- **18-bit page number**
- **12-bit offset**

Diagram:
- **base/bound**
- **base**
- **bound**
- **page table**
Hybrid approach - paged segmented memory

What if each segment was rarely larger than 1Ki pages of 4Kbyte.

```
31  29  12  0
seg  18-bit page number  12-bit offset
```

```
base/bound

bound

page table

frame number

base
```
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</table>

- **seg**: 32-bit segment number
- **18-bit page number**: 18-bit page number
- **12-bit offset**: 12-bit offset

- **base**: Pointer to base of segment
- **bound**: Pointer to bound of segment
- **page table**: Page table
- **frame number**: Frame number
Hybrid approach - paged segmented memory

What if each segment was rarely larger than 1Ki pages of 4Kibyte.

```
seg  18-bit page number  12-bit offset
| 31  |  29 |  12 |    |  0 |
```

- base/bound
- bound
- page table
- frame number
- base
- page
Multi-level page table

31

0
### Multi-level page table

<table>
<thead>
<tr>
<th>31</th>
<th>22</th>
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</tr>
</thead>
<tbody>
<tr>
<td>10-bit directory index</td>
<td></td>
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</table>
# Multi-level page table

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- **Page directory**: A structure used to map virtual memory addresses to physical memory addresses. It contains a list of entries, each of which points to a page frame in physical memory.

- **Page table**: A data structure used to map virtual memory addresses to page frames. Each entry in the page table points to a page frame in the page frame table.

- **Page frame**: A fixed-size block of physical memory used to store a program or data. Each page frame is associated with a unique virtual address block.
Multi-level page table

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page directory
Multi-level page table

31  22  12  0
10-bit directory index  10-bit page index  12-bit offset

page directory

page table
Multi-level page table

<table>
<thead>
<tr>
<th>31</th>
<th>22</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-bit directory index</td>
<td>10-bit page index</td>
<td>12-bit offset</td>
<td></td>
</tr>
</tbody>
</table>

page directory → page table
Multi-level page table

- 10-bit directory index
- 10-bit page index
- 12-bit offset

Diagram:
- Page directory
- Page table
- Page
Multi-level page table

- 10-bit directory index
- 10-bit page index
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Diagram:
- Page directory
- Page table
- Page
page directory

virtual address space
Mostly empty space

page directory

virtual address space
Mostly empty space

page directory

virtual address space
Mostly empty space

- Page directory
- Virtual address space
Mostly empty space

page directory

virtual address space
Mostly empty space

page directory

each page table can map 4 Mibyte

virtual address space
More than two levels

Scheme used in PAE, where each entry has a 24-bit physical base address.

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
More than two levels

31

2-bit page global directory index
More than two levels

Scheme used in PAE, where each entry has a 24-bit physical base address.

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
More than two levels

Scheme used in PAE, where each entry has a 24-bit physical base address.

Trace the translation of a 32-bit virtual address to a 36-bit physical address.

2-bit page global directory index

9-bit page middle directory index

9-bit page table index
More than two levels

<table>
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<th>29</th>
<th>2120</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
</table>

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- 9-bit page table index
- 2-bit page global directory index
- 12-bit offset

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*Scheme used in PAE, where each entry has a 24-bit physical base address.*

Trace the translation of a 32-bit virtual address to a 36-bit physical address.
Linux on x86_64 architectures

- A 64-bit address but only 48-bits are used.
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- Bits 63-47 are either 1, kernel space, or 0, user space.
- The 48 bits are divided into:
  - 9-bit page global directory index
  - 9-bit page upper directory index
  - 9-bit page lower directory index
  - 9-bit page table index
  - 12-bit offset

- A page table entry is 8 bytes and contains a 40-bit physical address base address.
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A page table entry is 8 bytes and contains a 40-bit physical address base address.

The 40-bit base is combined with the 12-bit index to a 52-bit physical address.
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Inverted page tables

Why not do something completely different?

We will probably not have more than say 8 Gibyte of main memory.

If we divide this into 4 Kibyte frames we have 2 Mi frames.

Assume maintain a table with 2 Mi entries that describes which process and page that occupies the frame.

To translating a virtual address we simply search the table (efficient if we use a hash table).

Used by some models of PowerPC, Ultra Sparc and Itanium.
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Summary

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- Small fixed size pages is a solution.
- Speed of translation is a problem (what is the solution?)
- The size of the page table is a problem (and you know how to solve it).
- Inverted page tables - an alternative approach.
TLB - dynamite, makes paging possible.