

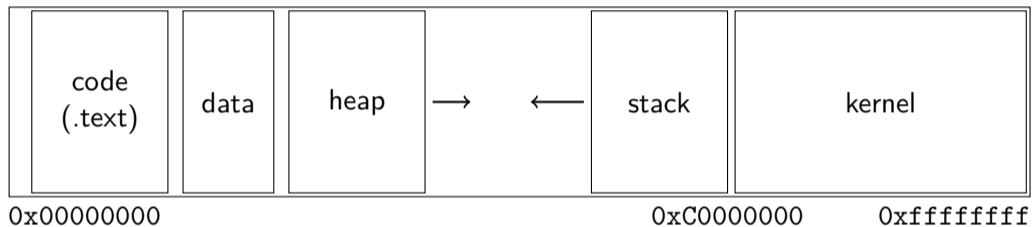
Memory

Johan Montelius

KTH

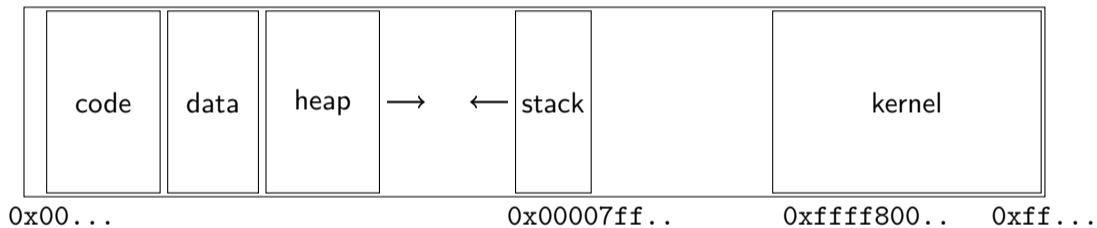
2021

The process

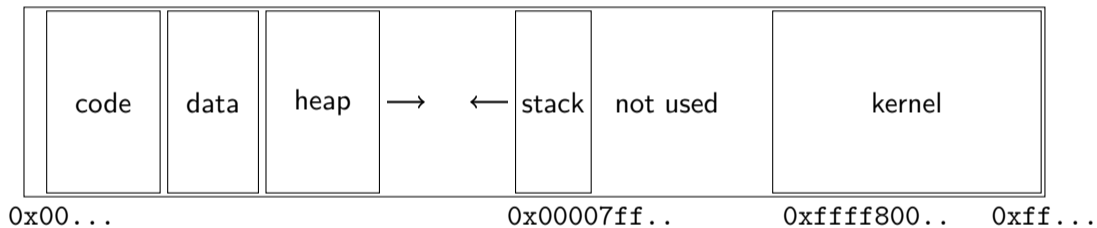


Memory layout for a 32-bit Linux process

64-bit Linux on a x86_64 architecture



64-bit Linux on a x86_64 architecture



Memory virtualization

Every process has an address space from zero to some maximal address.

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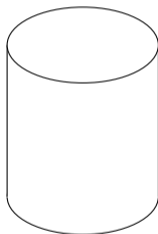
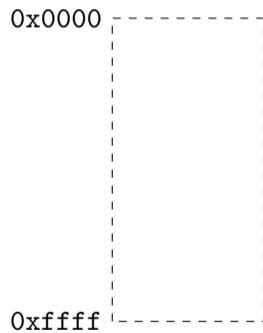


IBM System 360

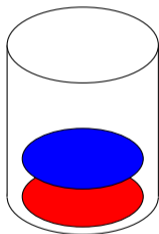
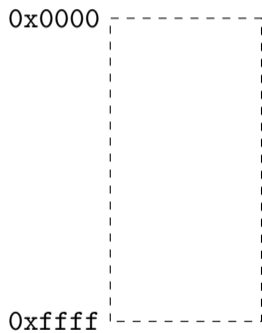
- 1964, 8-64 Kbyte memory
- 12+12 bit address space
- batch operating system

Chief architect: Gene Amdahl

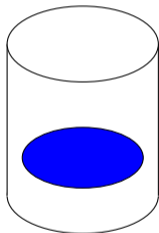
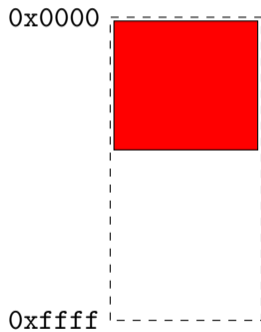
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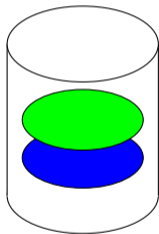
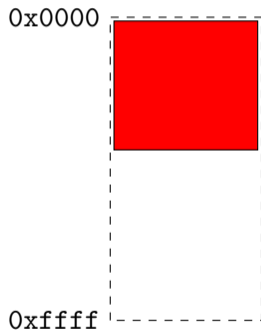
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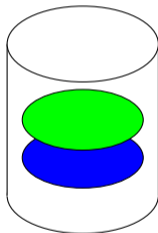
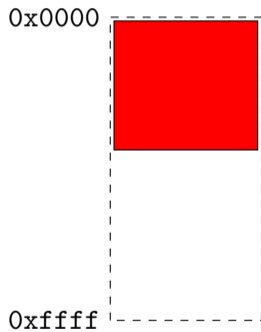
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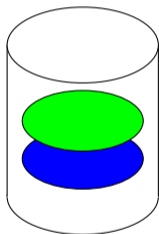
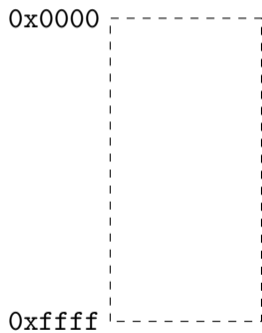
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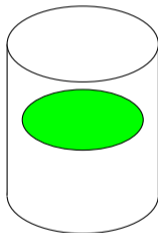
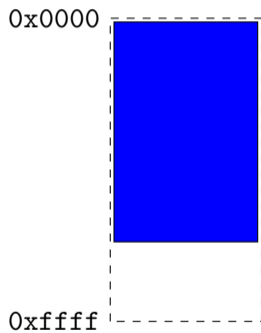
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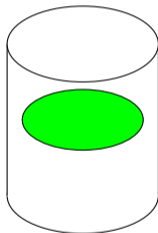
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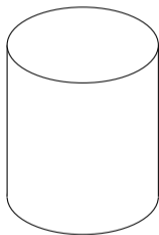
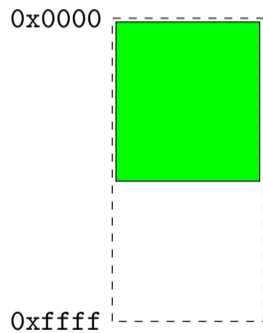
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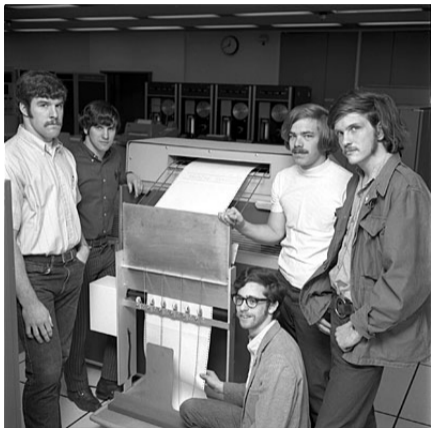


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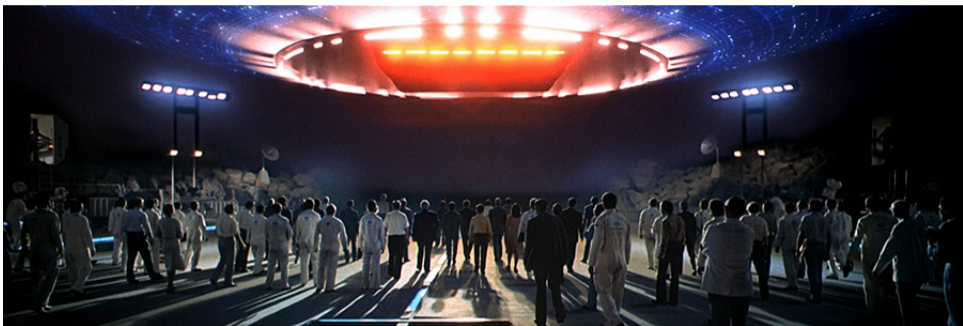




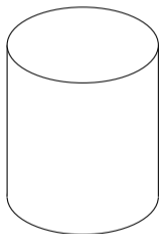
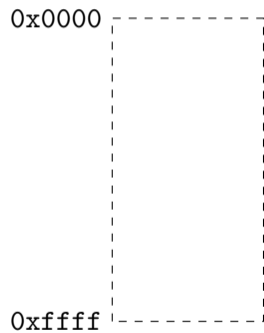
GE-235

- 1964
- 20-bit word
- 8 Kword address space

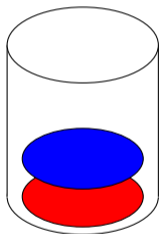
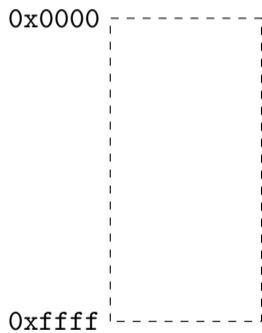
Arnold Spielberg was in the team that designed the GE-235



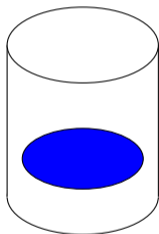
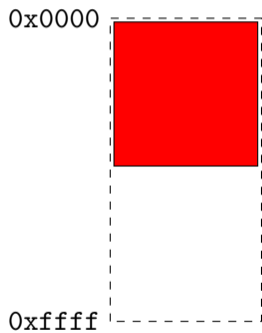
Time-sharing:



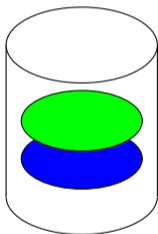
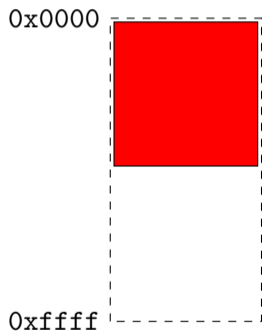
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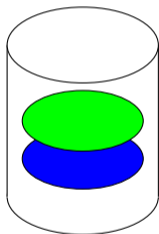
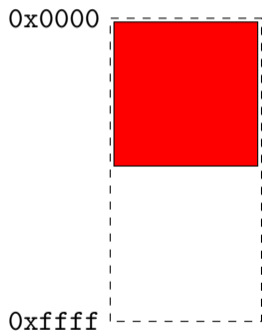
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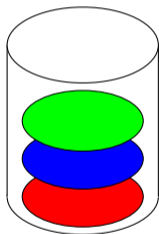
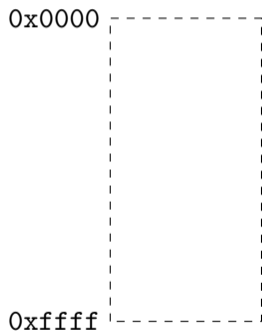
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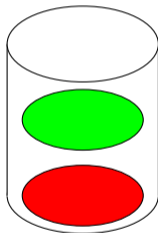
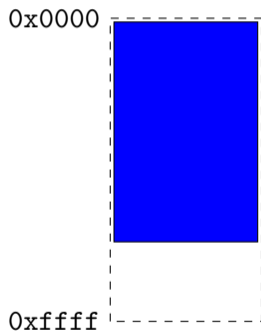
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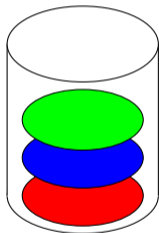
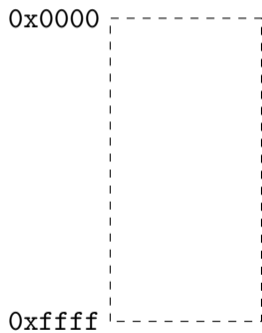
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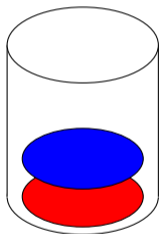
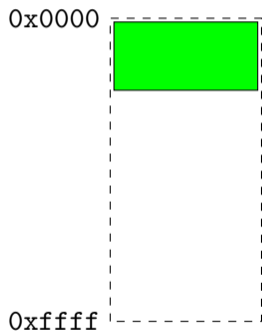
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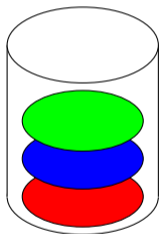
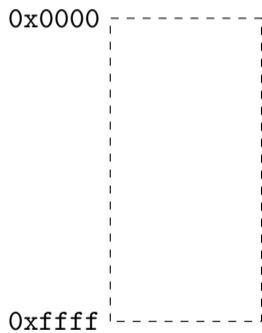
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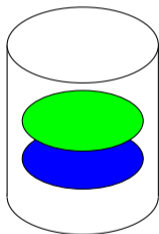
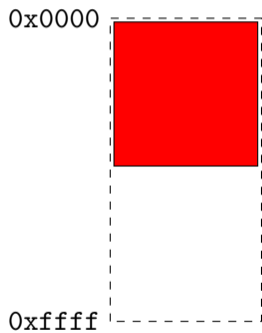
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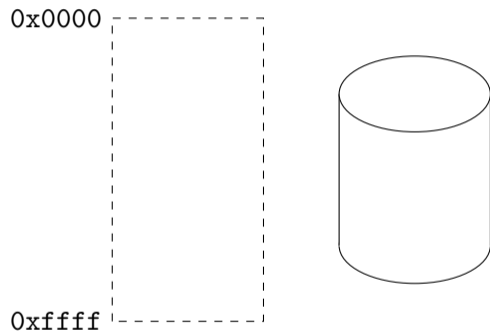


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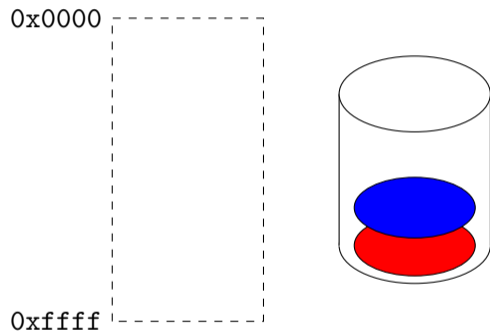
why not switch between two programs

If both programs will fit in memory:



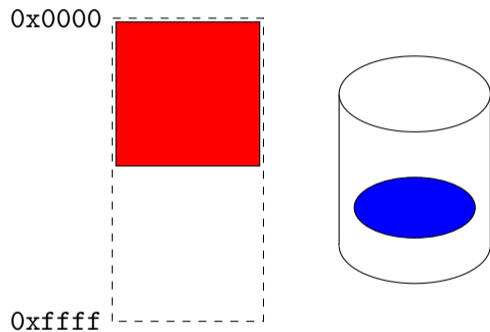
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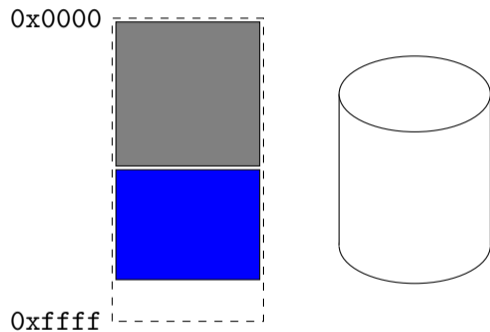
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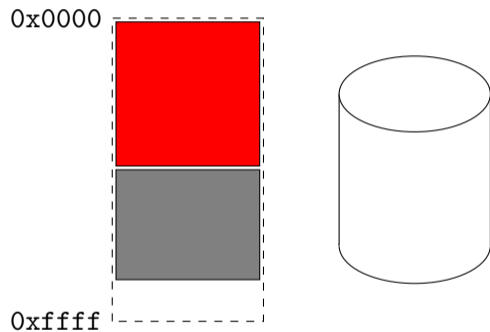
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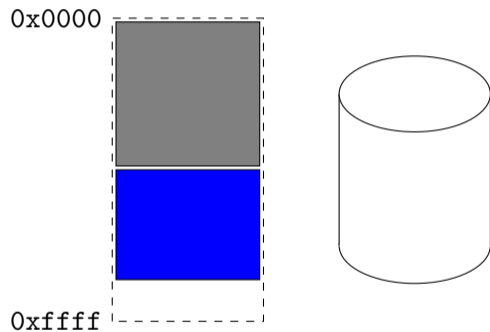
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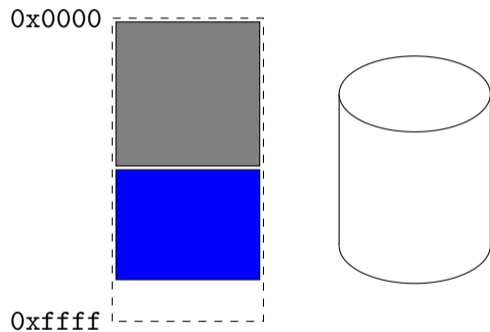
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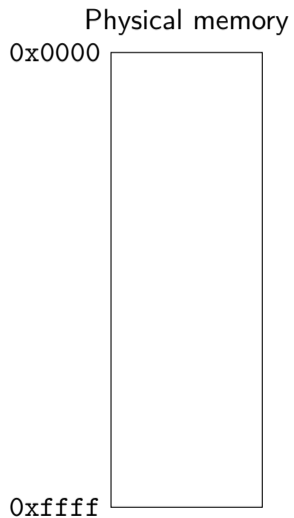
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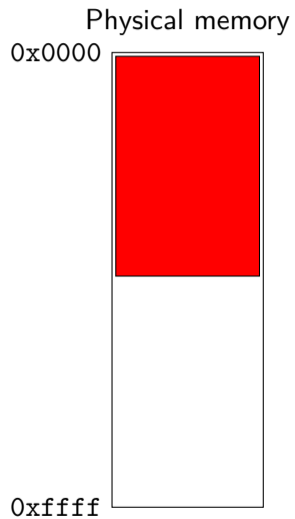


What is the problem?

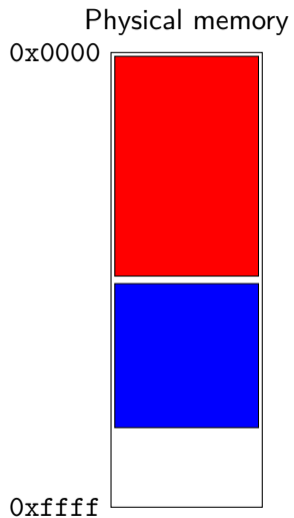
Virtual memory



Virtual memory

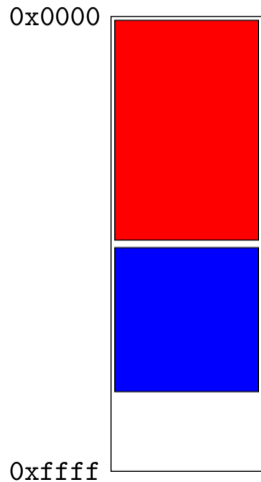


Virtual memory



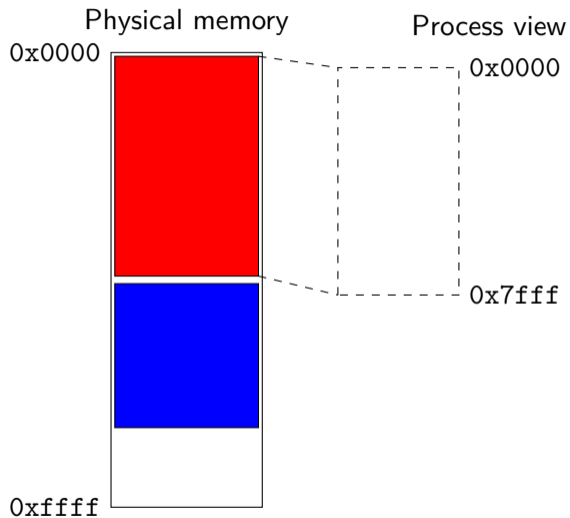
Virtual memory

Physical memory

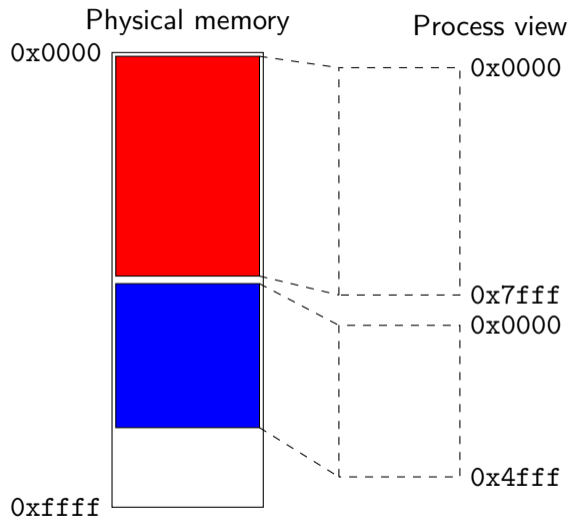


Process view

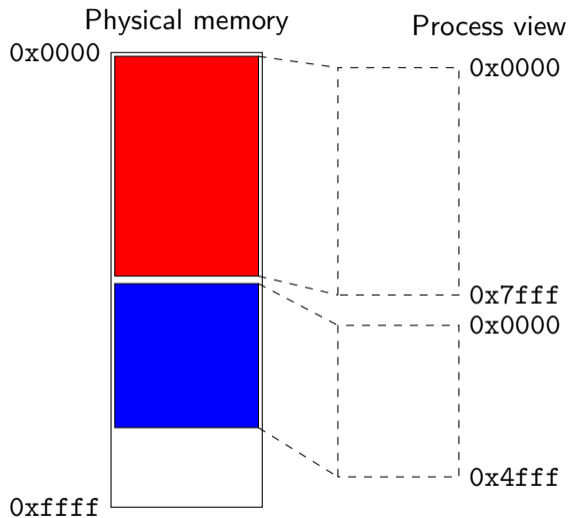
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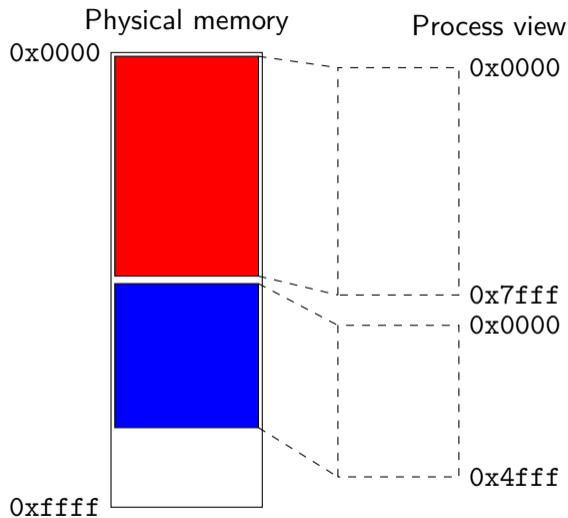


Virtual memory



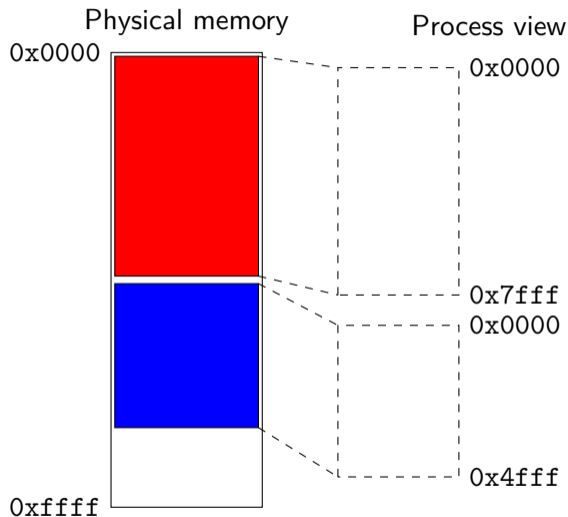
- Transparent: processes should be unaware of virtualization.

Virtual memory



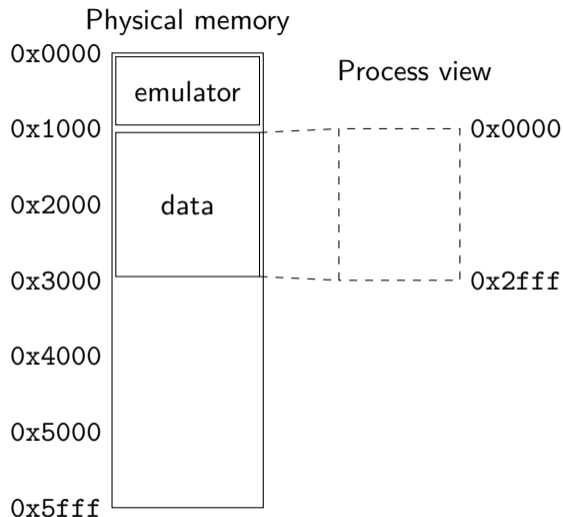
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Virtual memory



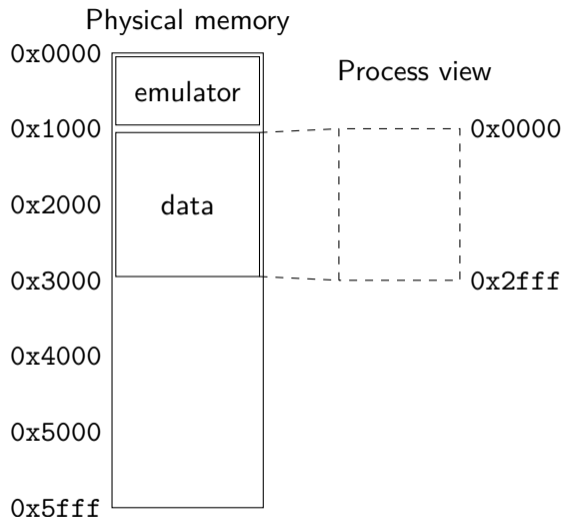
- Transparent: processes should be unaware of virtualization.
- Protection: processes should not be able to interfere with each other.
- Efficiency: execution should be as close to real execution as possible.

Emulator - simple but slow



Let the operating system run an *emulator* that interprets the operations of the process and changes the memory addresses as needed.

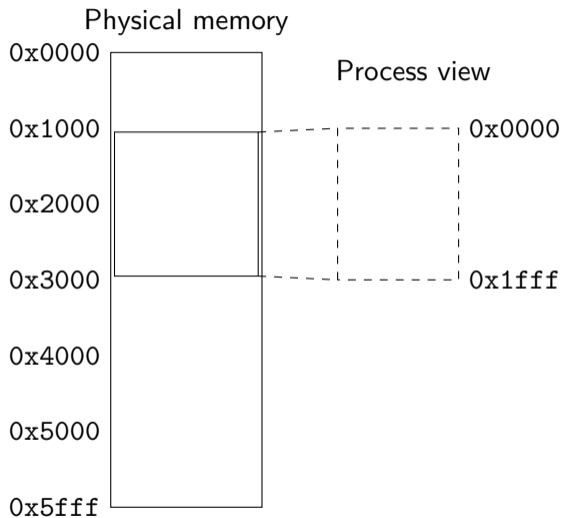
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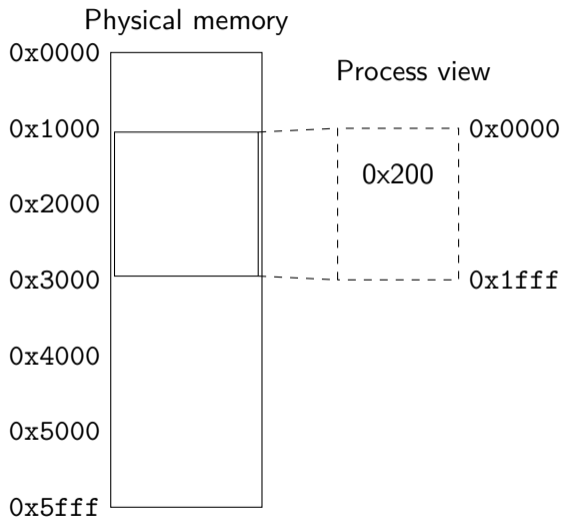
This is similar to how the JVM works

Static relocation - ehj, static



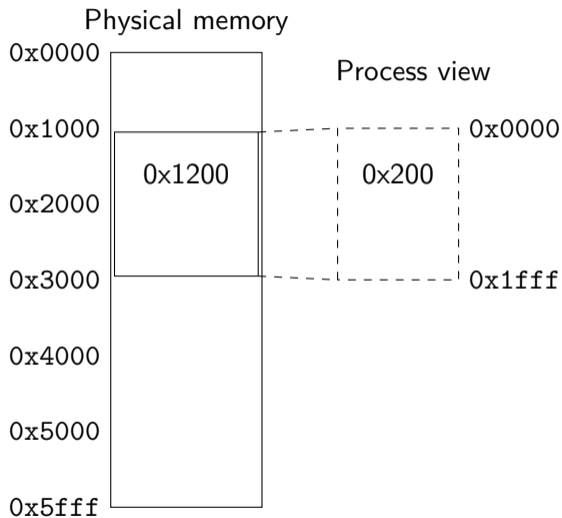
When a program is loaded, all references to memory locations are changed so that they correspond to the actual location in RAM where the program is loaded.

Static relocation - ehj, static



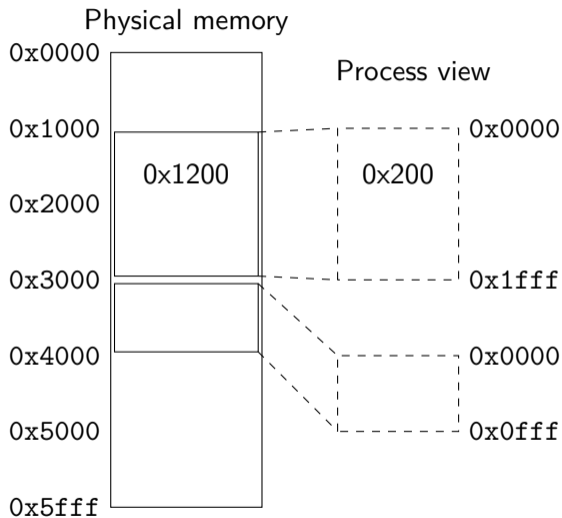
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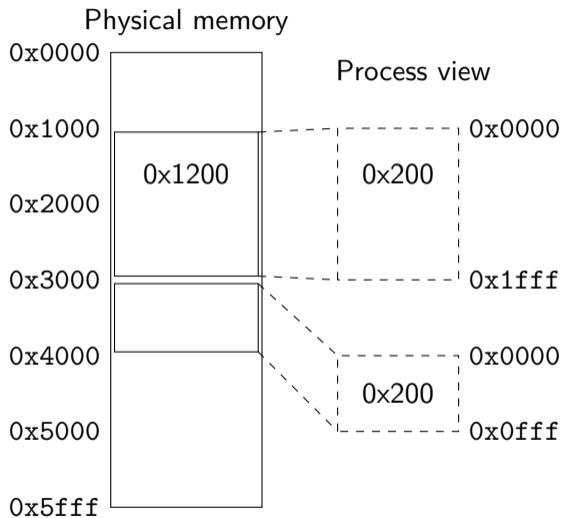
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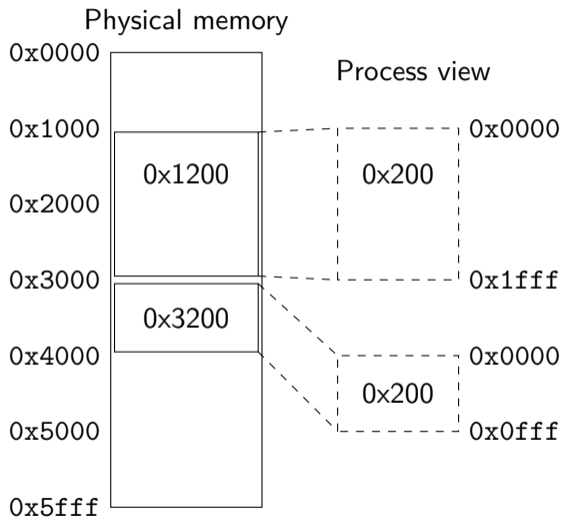
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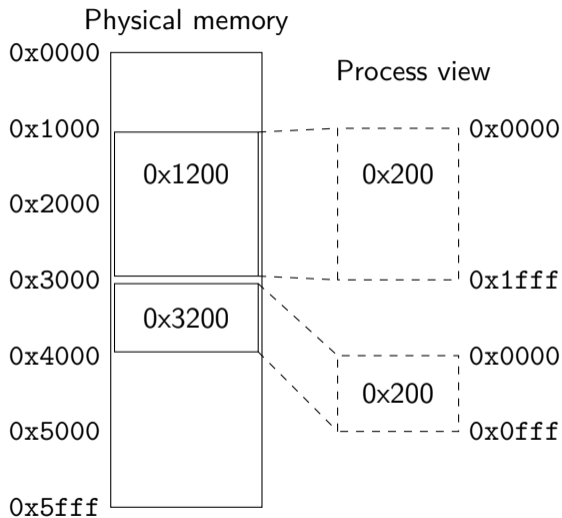
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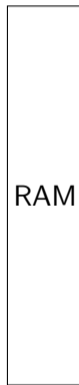


When a program is loaded, all references to memory locations are changed so that they correspond to the actual location in RAM where the program is loaded.

How do we know we have changed all addresses?

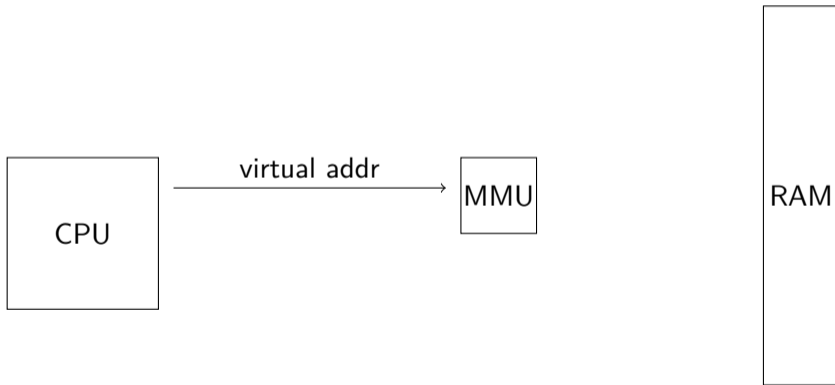
Dynamic relocation

Change every memory reference, on the fly, to a region in memory allocated for the process.



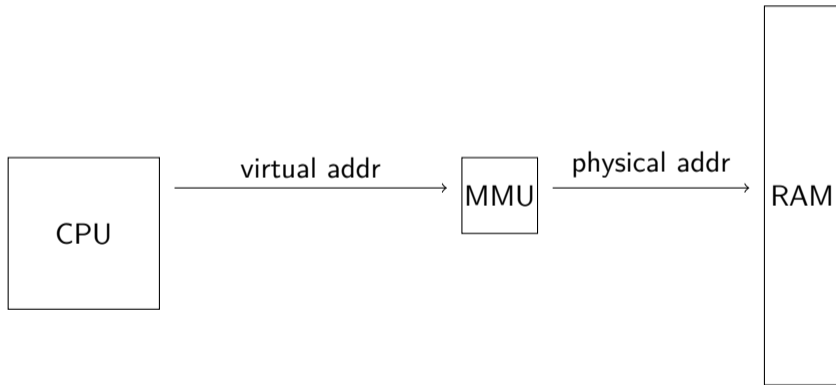
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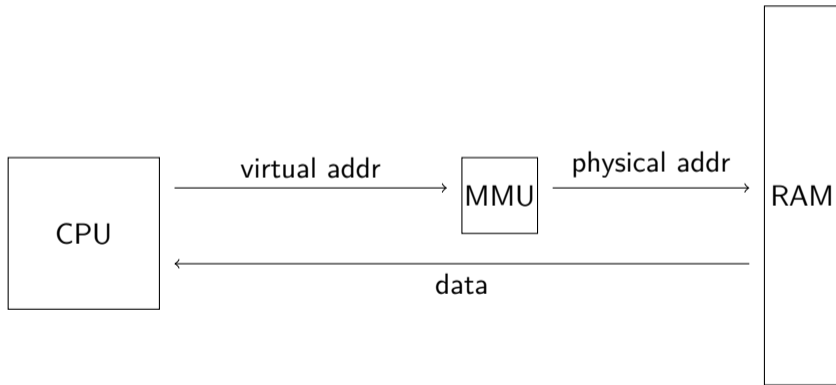
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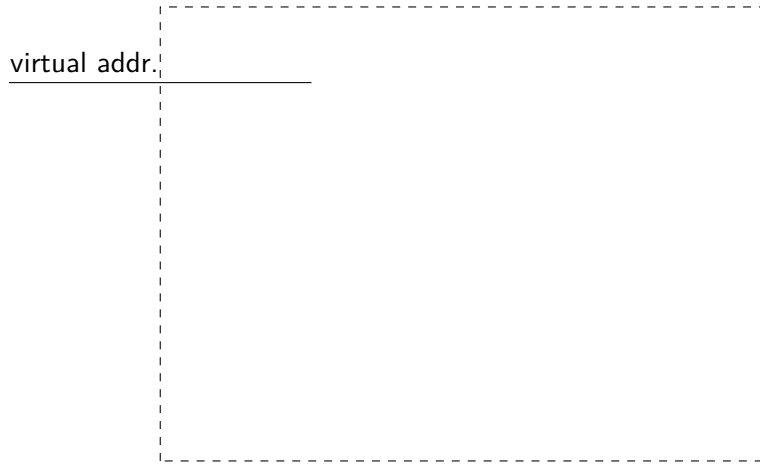
Dynamic relocation

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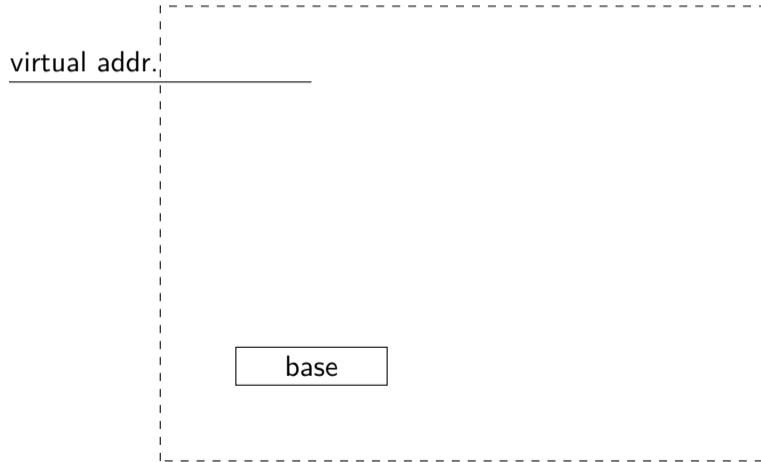


MMU

virtual addr.

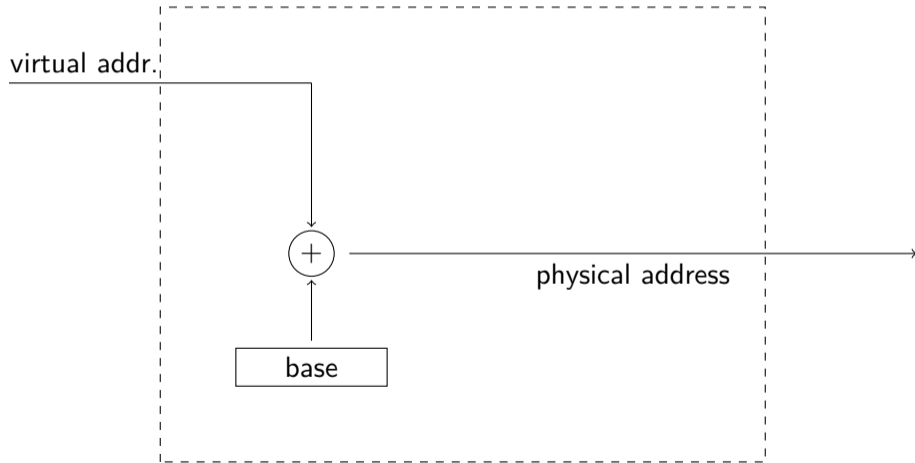
A diagram illustrating the MMU virtual address structure. A horizontal line labeled "virtual addr." is shown on the left. This line extends into a large dashed rectangular box that represents the MMU's address space. The line is positioned at the top of the box, indicating the starting point of the virtual address within the MMU's mapping.

MMU



Base register

MMU



Base problem

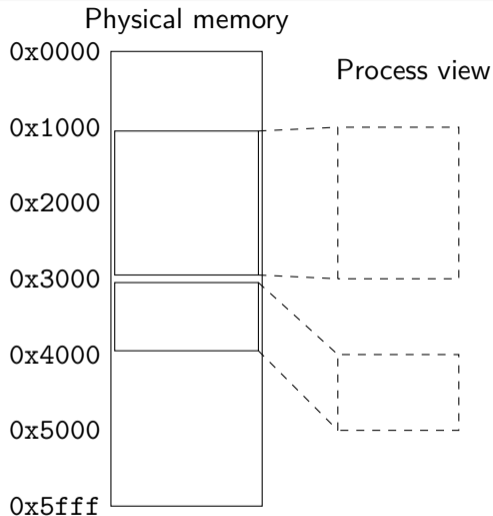
- Who is allowed to change the base register?

Base problem

- Who is allowed to change the base register?
- How do we prevent one process from overwriting another process?

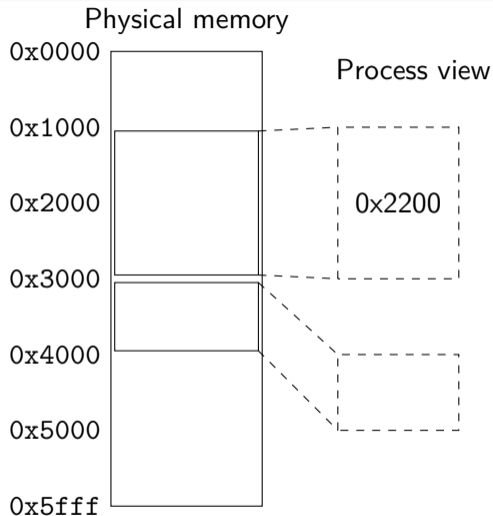
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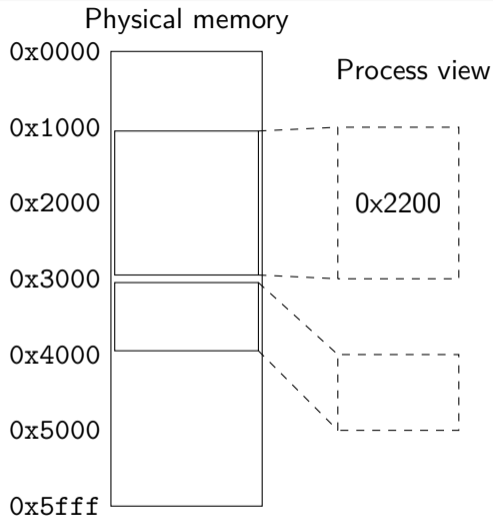
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- How do we prevent one process from overwriting another process?



Base problem

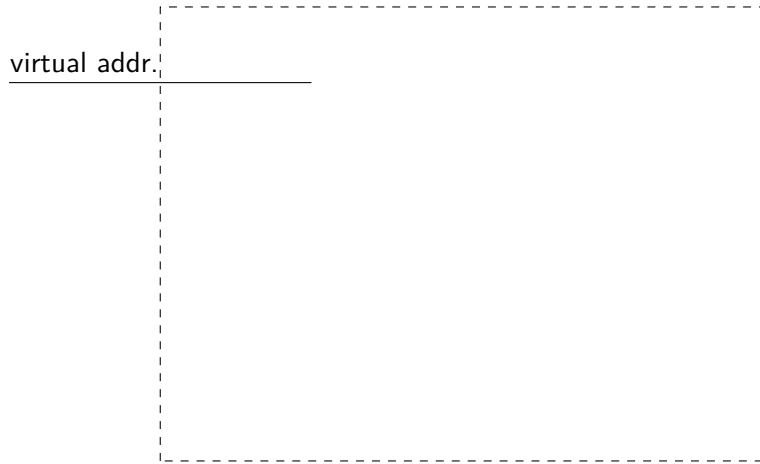
- Who is allowed to change the base register?
- How do we prevent one process from overwriting another process?



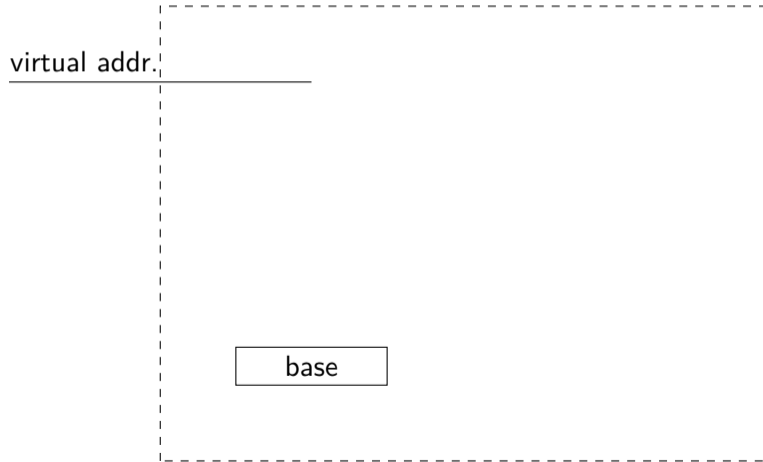
Can we prevent this at compile or load time?

MMU

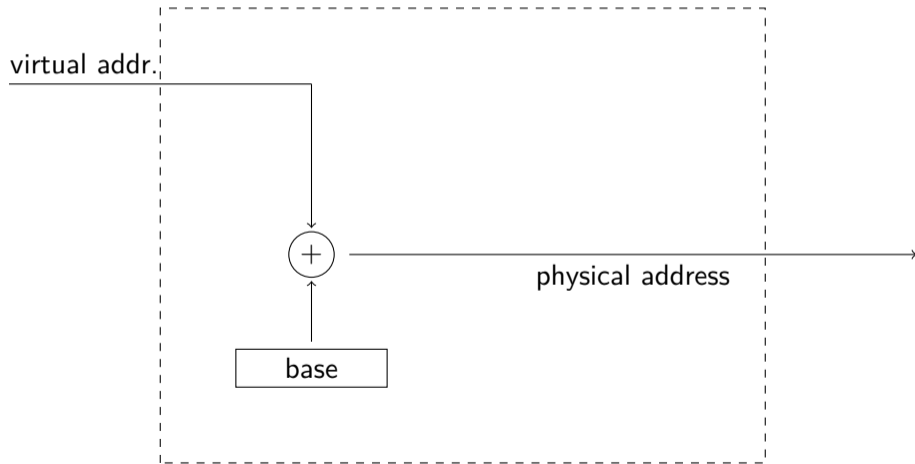
virtual addr.

A diagram illustrating the MMU process. A horizontal line labeled "virtual addr." points to a large dashed rectangular box, representing the virtual address space.

MMU

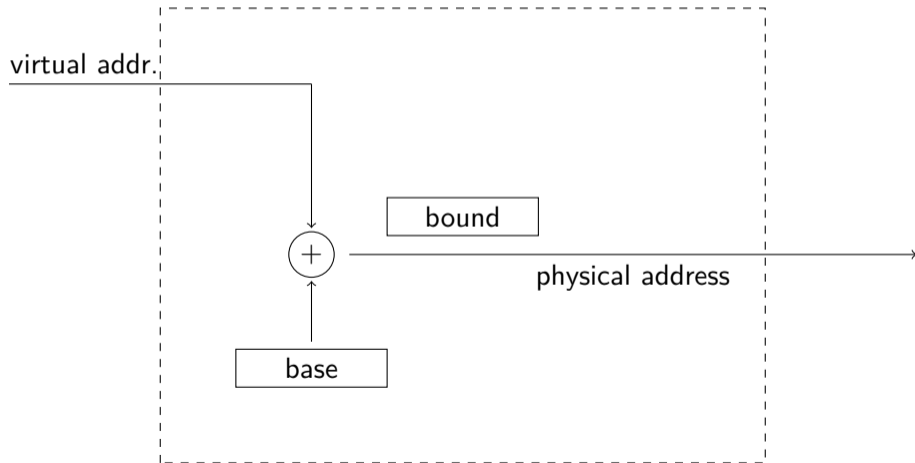


MMU



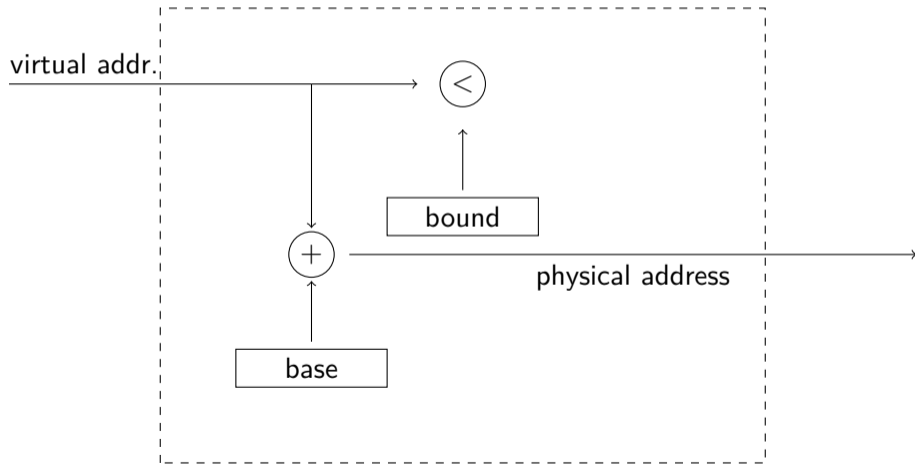
Base and bound

MMU



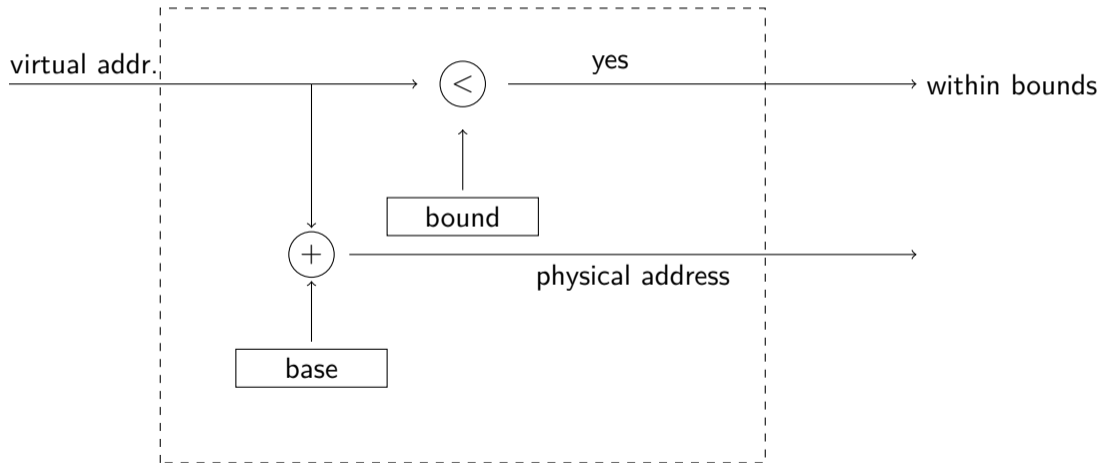
Base and bound

MMU

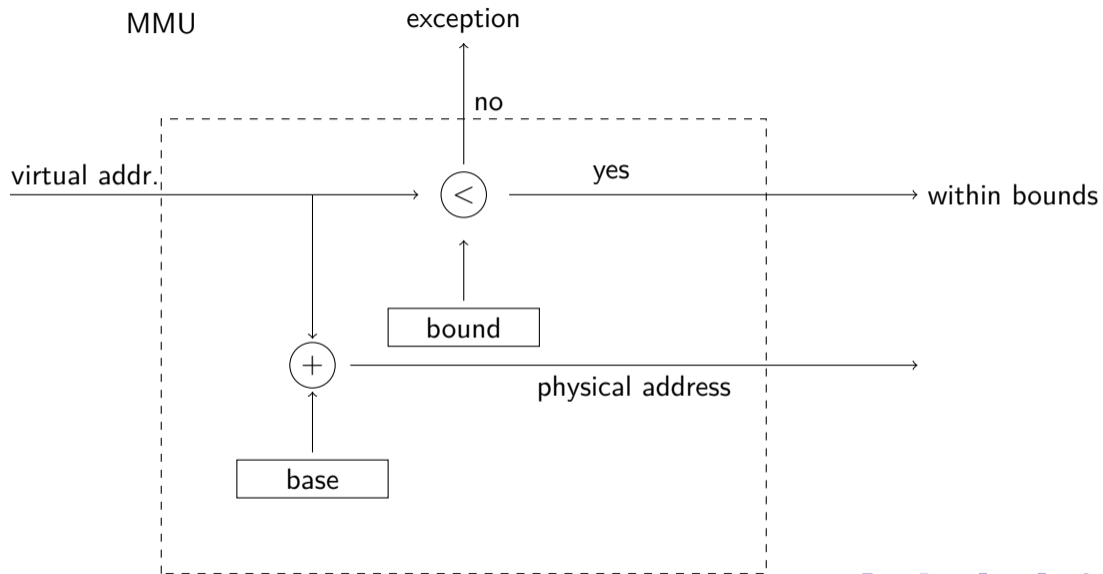


Base and bound

MMU



Base and bound



Pros:

- Transparent to a process.
- Simple to implement.
- Easy to change process.

Pros:

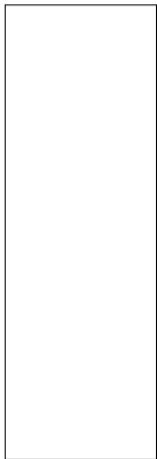
- Transparent to a process.
- Simple to implement.
- Easy to change process.

Cons:

- How do we share data?
- Wasted memory.

shared read-only segments

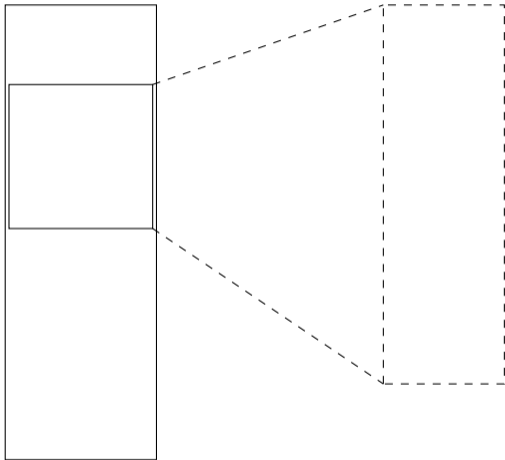
Physical memory



shared read-only segments

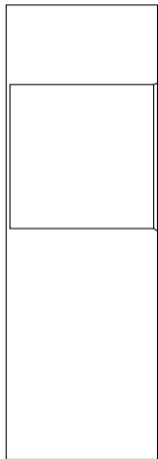
Physical memory

Process A

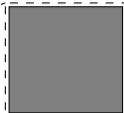


shared read-only segments

Physical memory

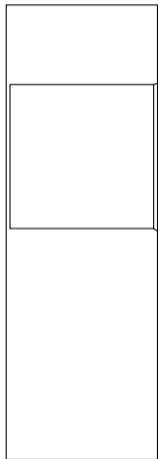


Process A

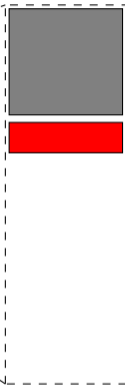


shared read-only segments

Physical memory

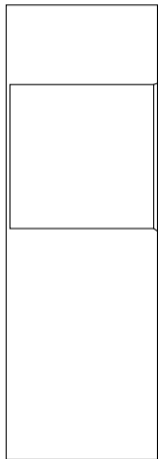


Process A

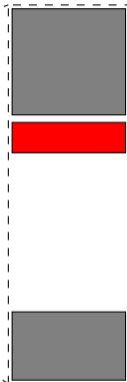


shared read-only segments

Physical memory

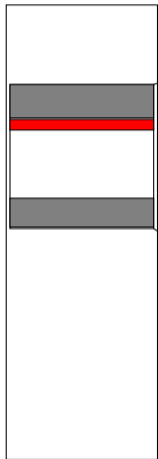


Process A

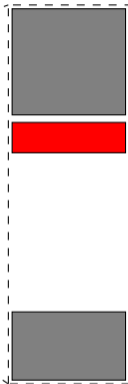


shared read-only segments

Physical memory

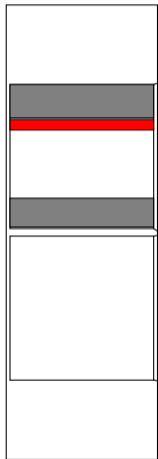


Process A

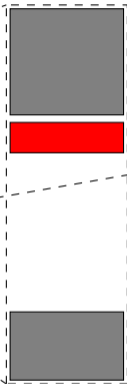


shared read-only segments

Physical memory



Process A

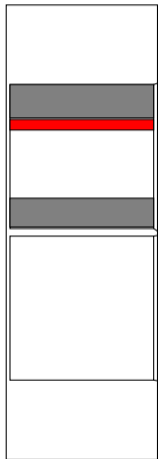


Process B

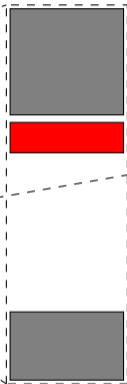


shared read-only segments

Physical memory



Process A

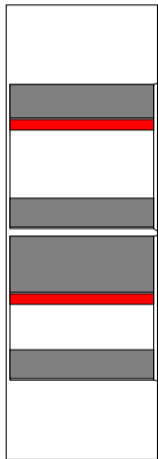


Process B

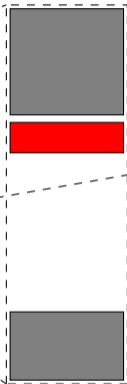


shared read-only segments

Physical memory



Process A

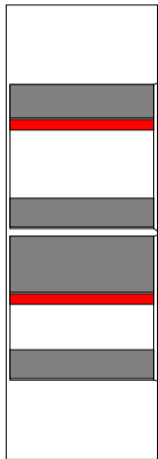


Process B

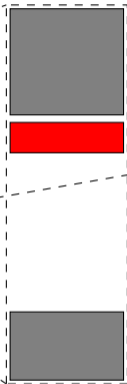


shared read-only segments

Physical memory



Process A



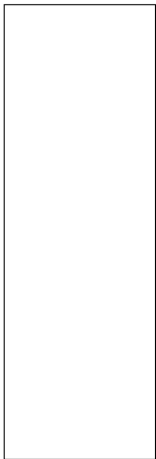
Process B



How do we write code that can be shared?

Internal fragmentation

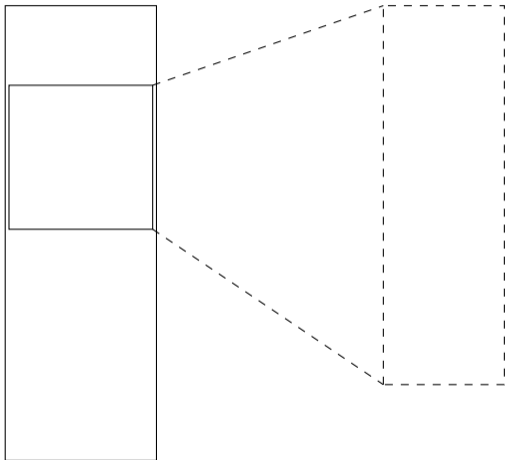
Physical memory



Internal fragmentation

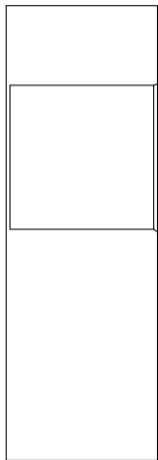
Physical memory

Process view



Internal fragmentation

Physical memory

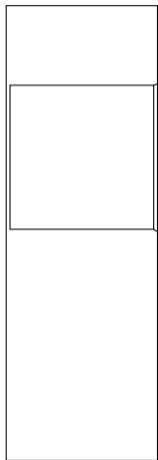


Process view



Internal fragmentation

Physical memory

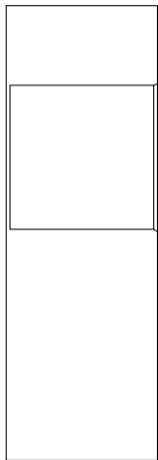


Process view



Internal fragmentation

Physical memory

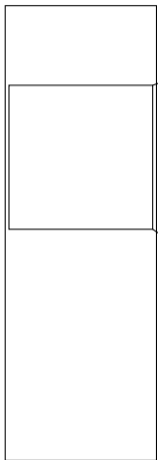


Process view

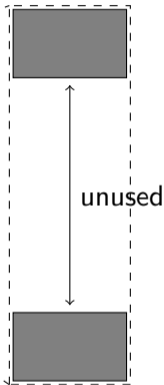


Internal fragmentation

Physical memory

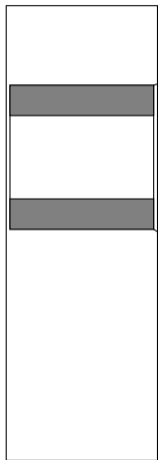


Process view

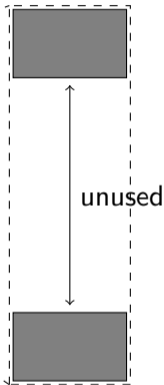


Internal fragmentation

Physical memory

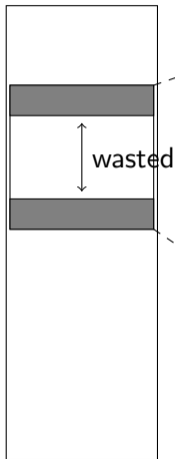


Process view

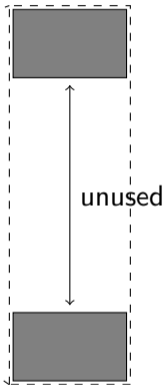


Internal fragmentation

Physical memory



Process view



Burroughs B5000



- 1961

Burroughs B5000



- 1961
- Designed for high-level languages:
ALGOL-60



- 1961
- Designed for high-level languages: ALGOL-60
- Memory access through a set of segment *descriptors* i.e. the view of a process is not a consecutive memory rather a set of individual memory segments.



- 1961
- Designed for high-level languages: ALGOL-60
- Memory access through a set of segment *descriptors* i.e. the view of a process is not a consecutive memory rather a set of individual memory segments.

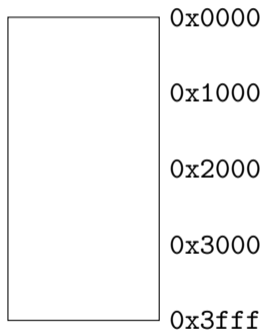
Donald Knuth was part of the design team.

```
procedure Absmax(a) Size:(n, m) Result:(y) Subscripts:(i, k);
  value n, m; array a; integer n, m, i, k; real y;

comment The absolute greatest element of the matrix a ...

begin
  integer p, q;
  y := 0; i := k := 1;
  for p := 1 step 1 until n do
    for q := 1 step 1 until m do
      if abs(a[p, q]) > y then
        begin y := abs(a[p, q]);
              i := p; k := q
        end
    end
  end
end Absmax
```

The view of the assembler programmer.



The view of the ALGOL programmer.

procedures

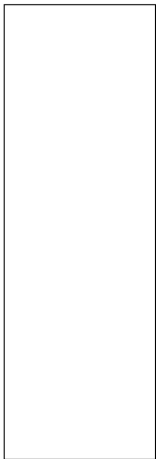


data



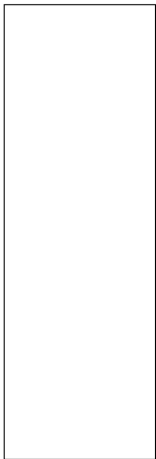
Segmented architecture

Physical memory



Segmented architecture

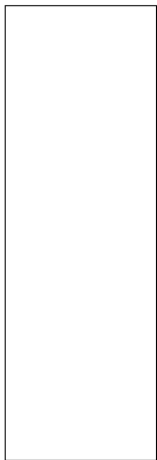
Physical memory



Process A

Segmented architecture

Physical memory

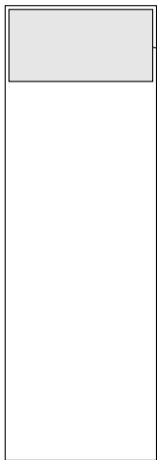


Process A



Segmented architecture

Physical memory

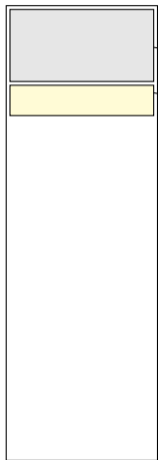


Process A



Segmented architecture

Physical memory



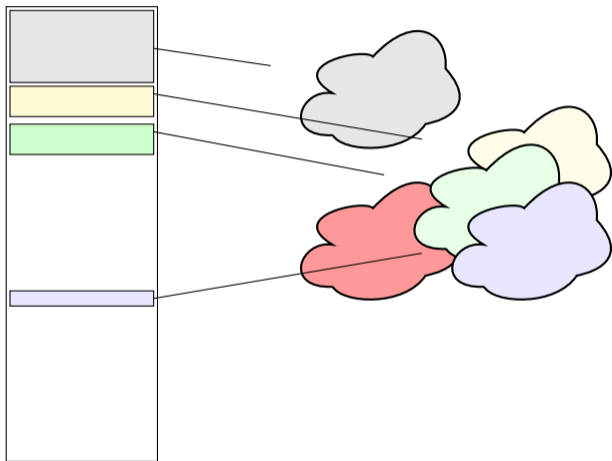
Process A



Segmented architecture

Physical memory

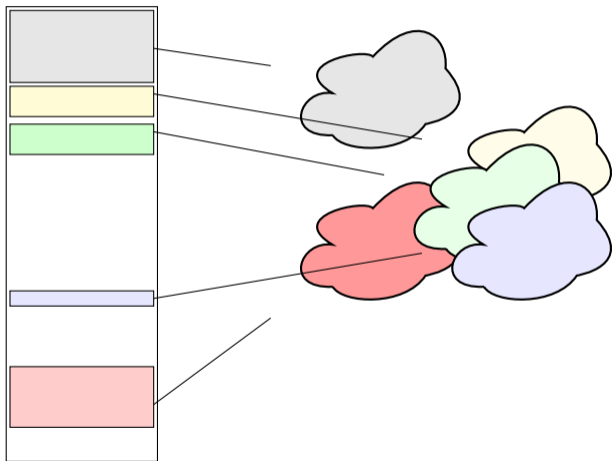
Process A



Segmented architecture

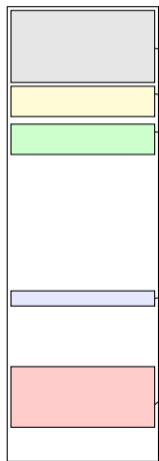
Physical memory

Process A



Segmented architecture

Physical memory



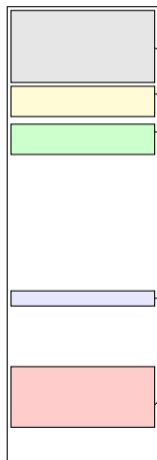
Process A



Process B

Segmented architecture

Physical memory



Process A

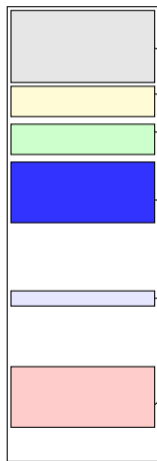


Process B

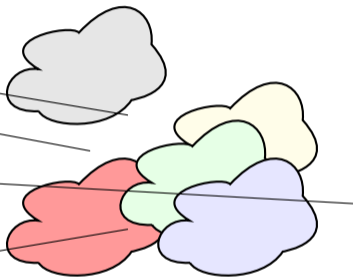


Segmented architecture

Physical memory



Process A

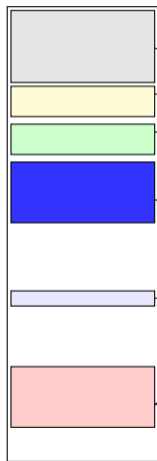


Process B

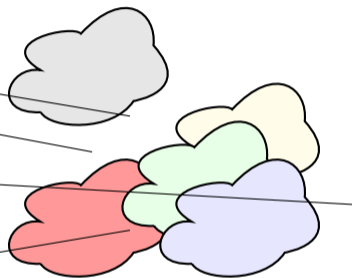


Segmented architecture

Physical memory



Process A



Process B

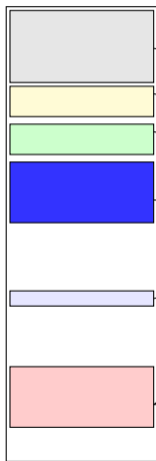


Segmented architecture

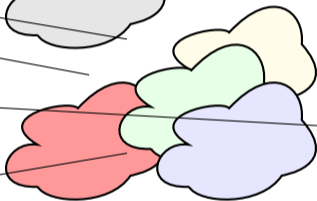
Physical memory

Process A

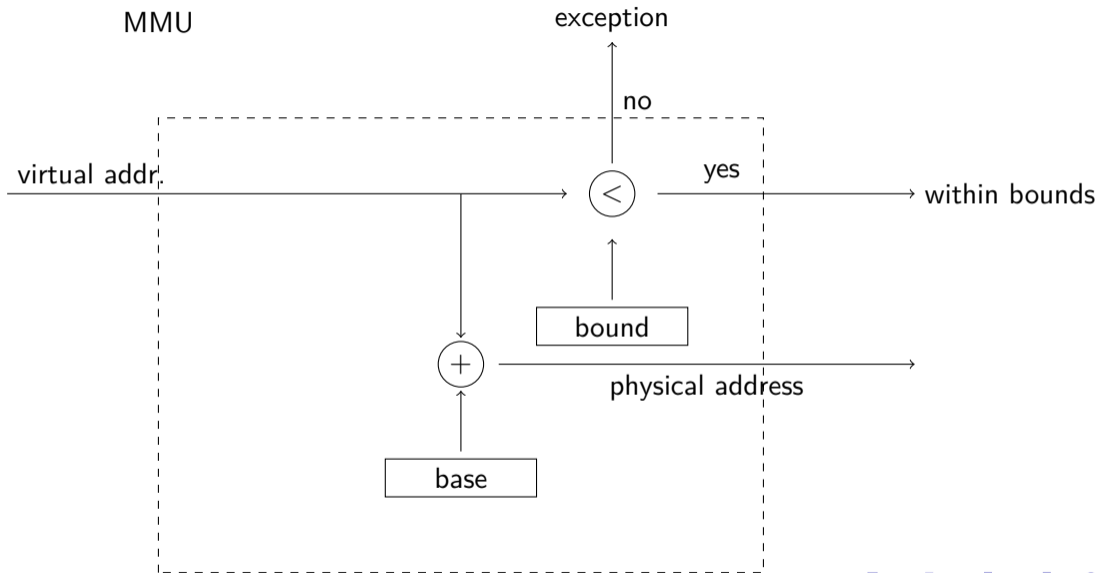
Process B



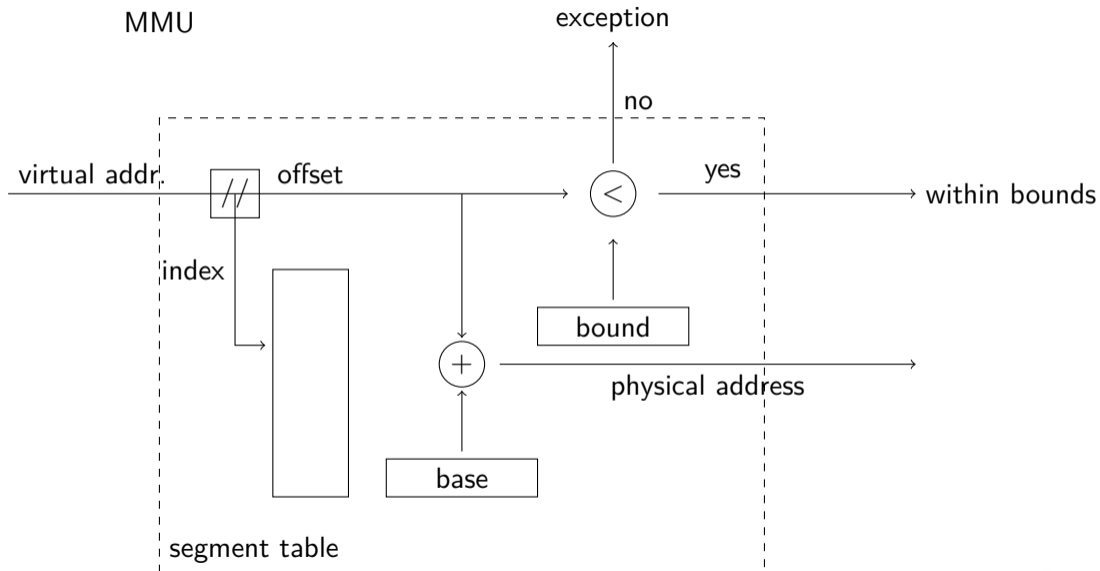
shared code



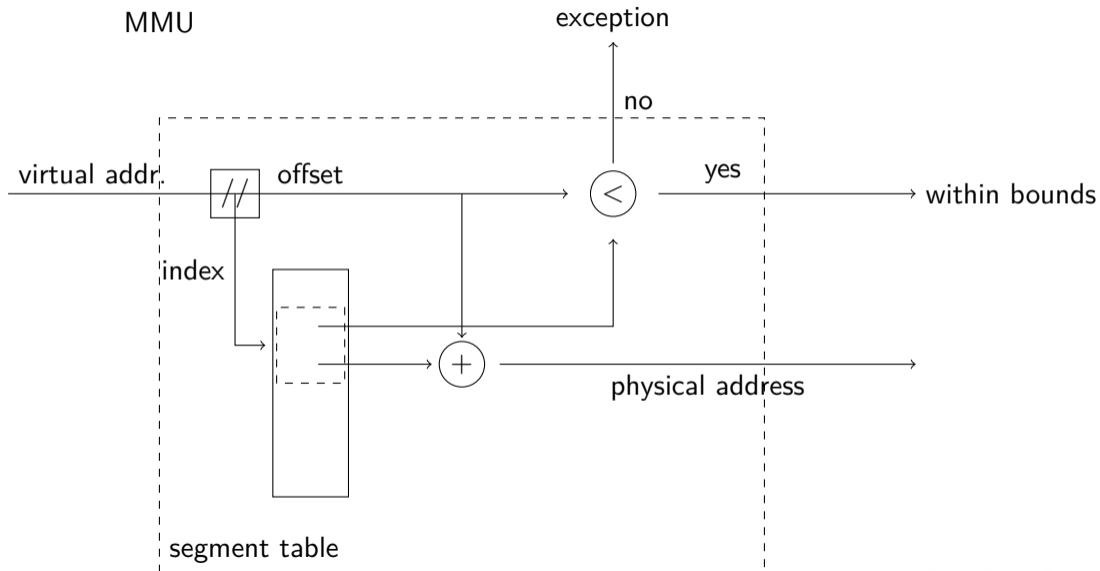
Segmented MMU

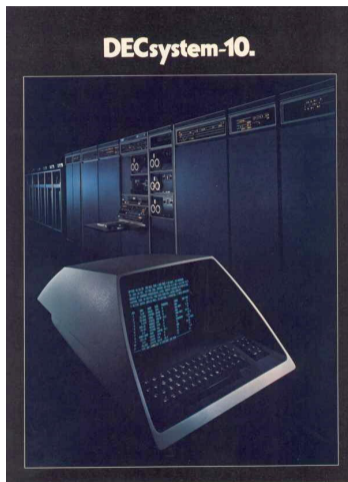


Segmented MMU



Segmented MMU



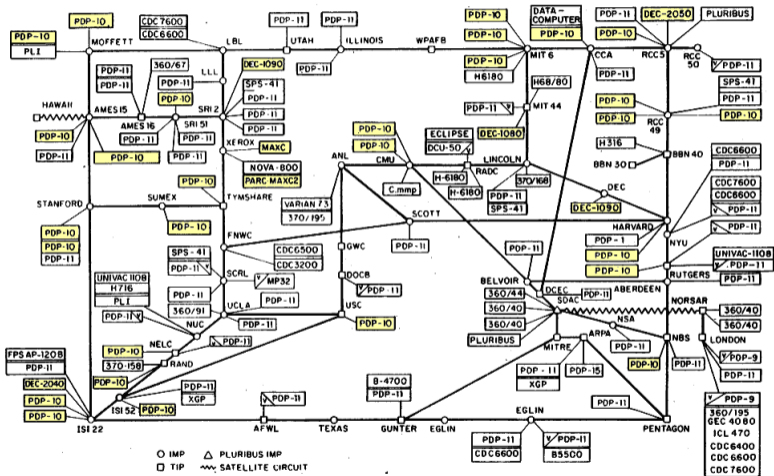


PDP-10

- 1966, 1 MHz
- 36 bit words
- 16 bit process address space (64Kword)
- 18 bit physical address (256 Kword)
- base and bound

The PDP10 had two segments per process, one read only code segment and one read/write for data.

ARPANET LOGICAL MAP, MARCH 1977



(PLEASE NOTE THAT WHILE THIS MAP SHOWS THE MOST POPULATION OF THE NETWORK ACCORDING TO THE BEST INFORMATION OBTAINABLE, NO CLAIM CAN BE MADE FOR ITS ACCURACY)

NAMES SHOWN ARE IMP NAMES, NOT (NECESSARILY) HOST NAMES

- Segments have variable size.



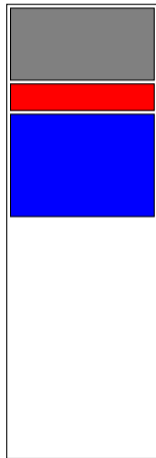
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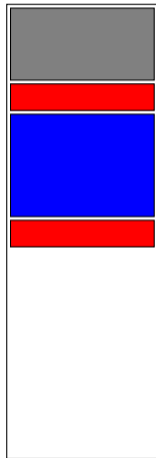
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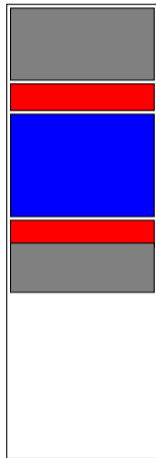
- Segments have variable size.



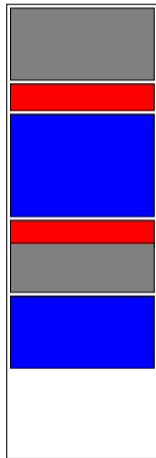
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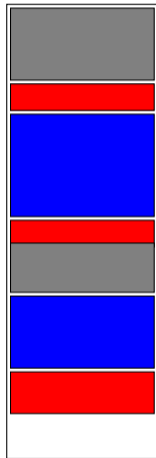
- Segments have variable size.



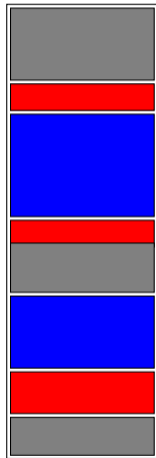
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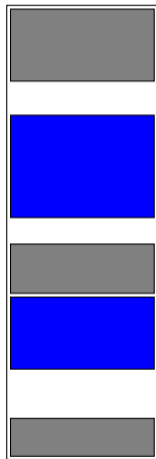


- Segments have variable size.



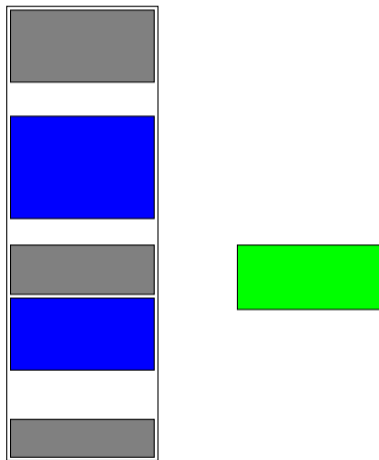
Segmentation: the solution

- Segments have variable size.
- Reclaiming segments will cause holes (external fragmentation).



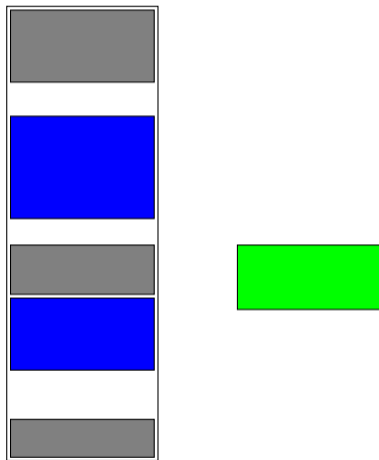
Segmentation: the solution

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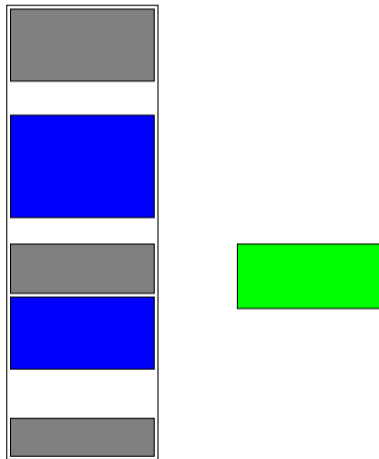
Segmentation: the solution - **not**

- Segments have variable size.
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- Compaction needed.



Segmentation: the solution - **not**

- Segments have variable size.
- Reclaiming segments will cause holes (external fragmentation).
- Compaction needed.



Is it possible to do compaction?

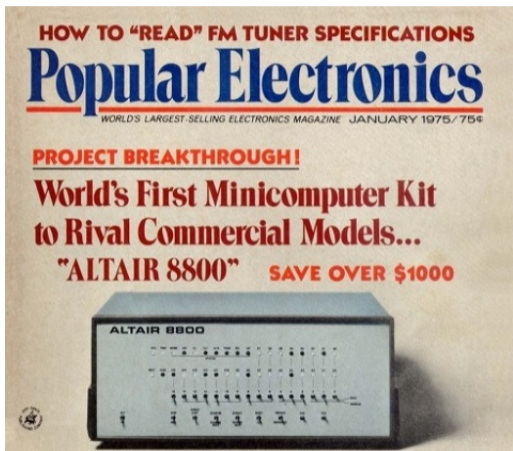
large grain vs fine grain segments

Using few large segments is easier to implement.

large grain vs fine grain segments

Using few large segments is easier to implement.

Using many small segments would allow the compiler and operating system to do a better job.



Intel 8080

- 1972
- 2 MHz
- 16 bit address space (64 Kbyte)

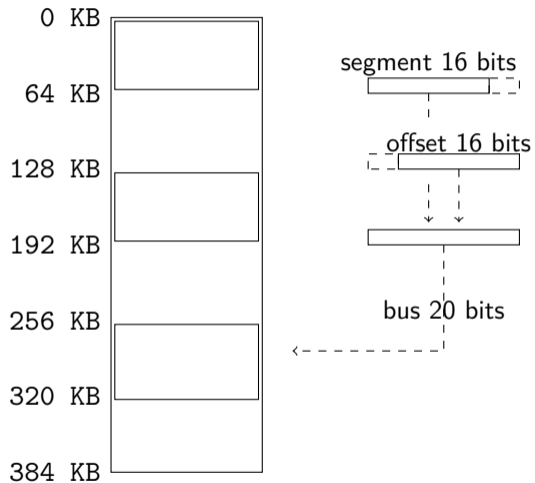
Altair 8800 would have 4 or 8 Kbytes of memory.



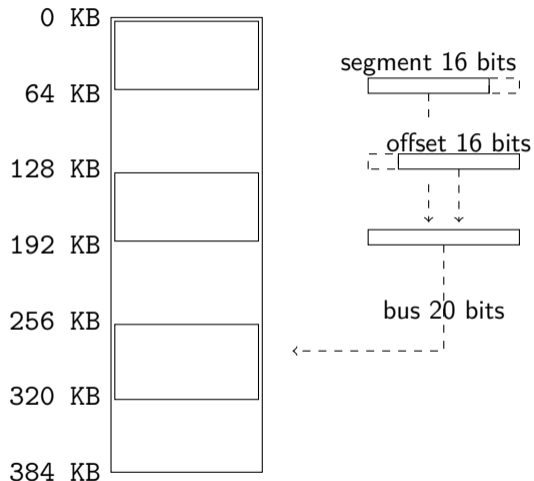
Intel 8086

- 1978, 5 MHz
- 16 bit address space (64 Kbyte)
- 20 bit memory bus (1 Mbyte)
- no protection of segments
- segments for: code, data, stack, extra

Segment addressing in 8086 - real mode

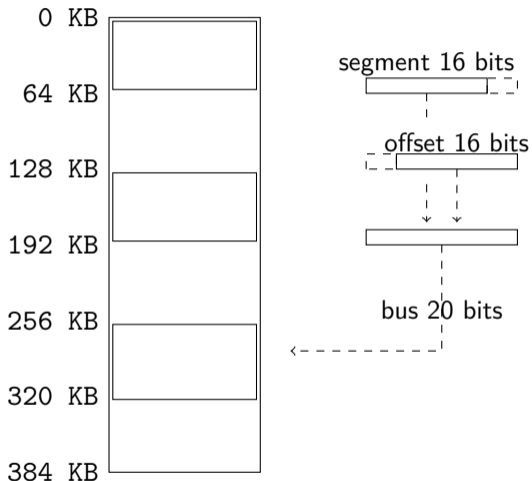


Segment addressing in 8086 - real mode



- Segment register chosen based on instruction: *code segment*, *stack segment*, *data segment* (and the *extra segment*).

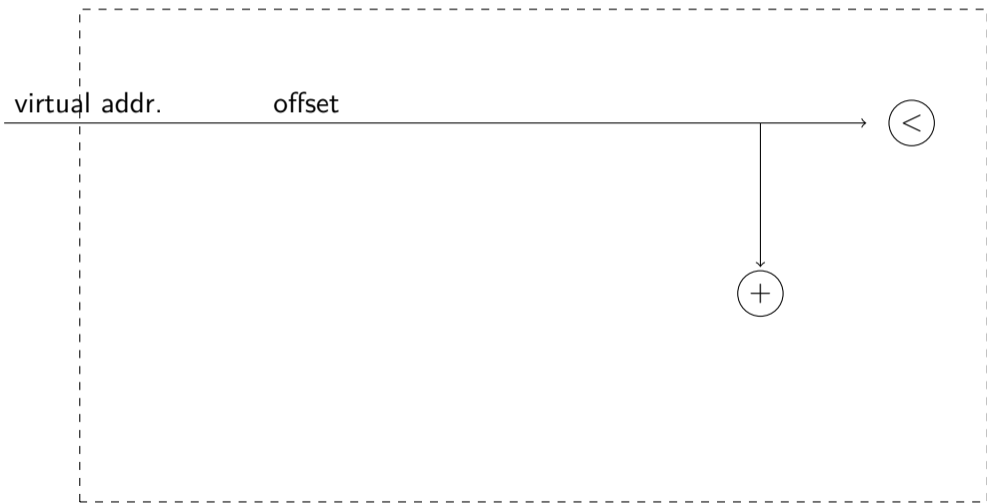
Segment addressing in 8086 - real mode



- Segment register chosen based on instruction: *code segment*, *stack segment*, *data segment* (and the *extra segment*).
- The segment architecture available still today in *real mode* i.e. the 16-bit mode that the CPU is initially in.

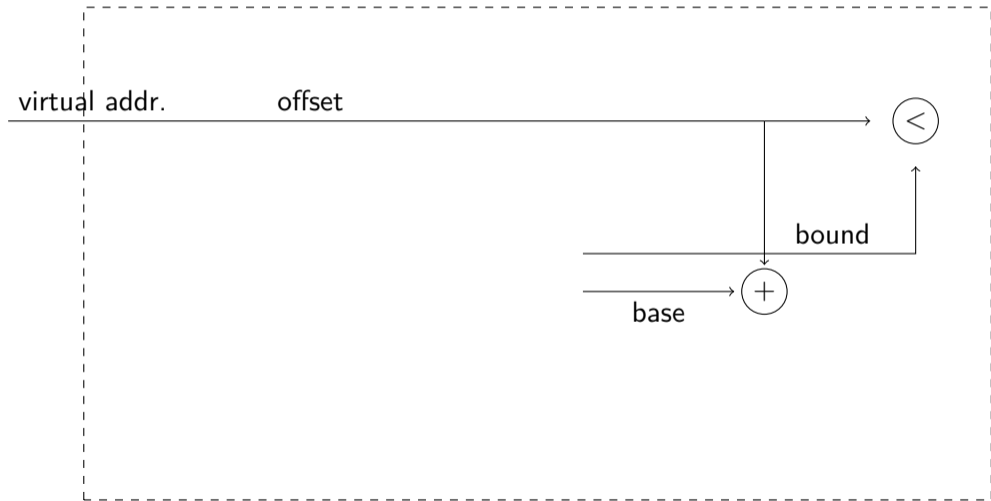
Segment addressing in 80386 - protected mode

MMU

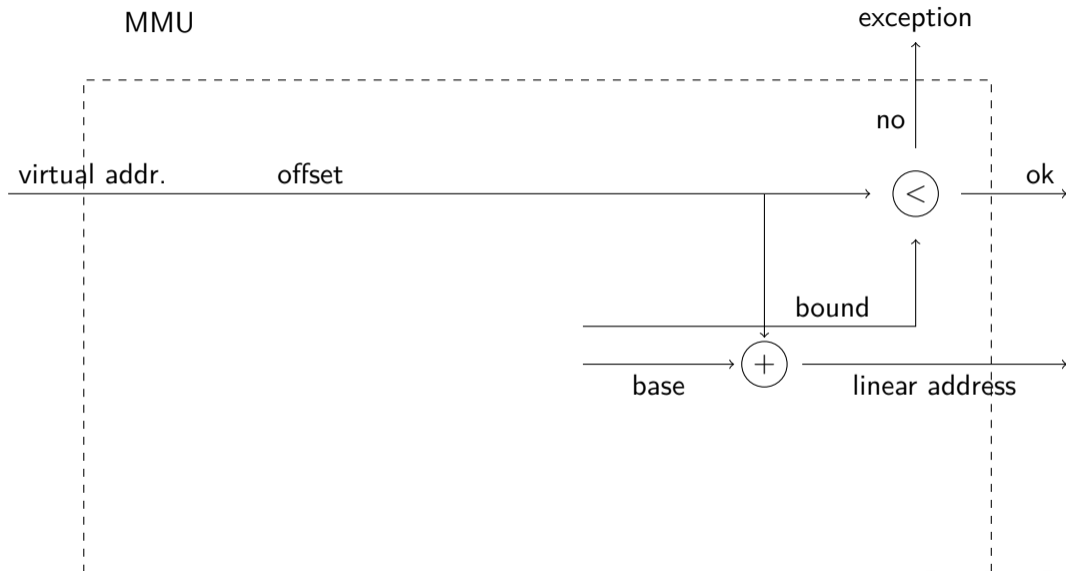


Segment addressing in 80386 - protected mode

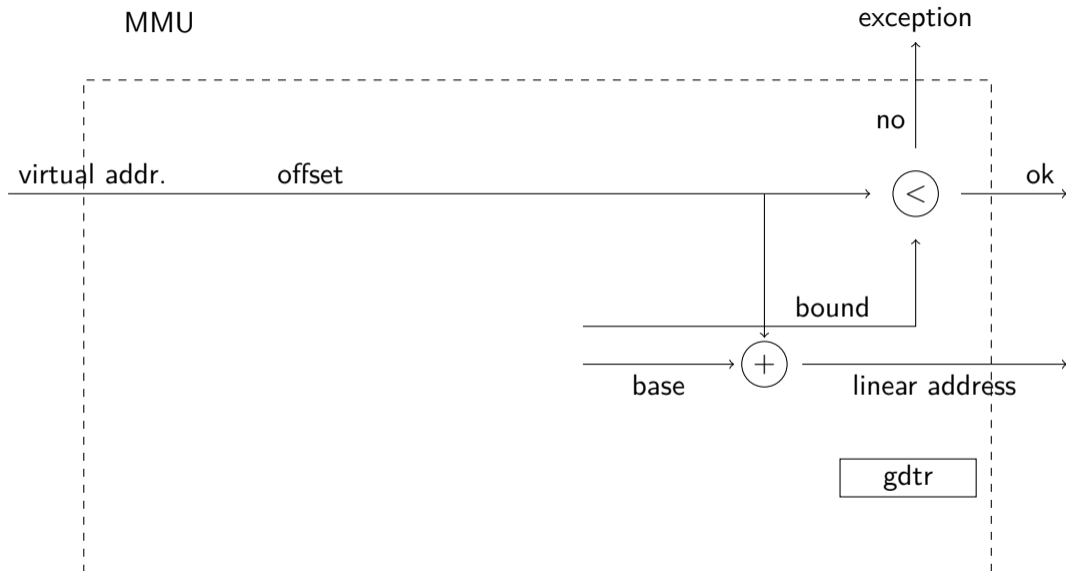
MMU



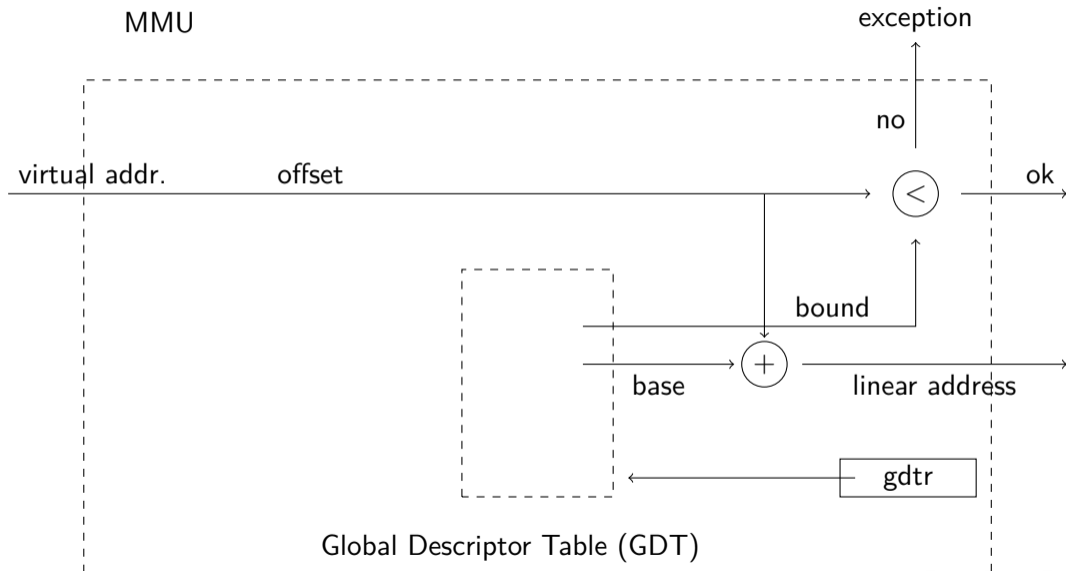
Segment addressing in 80386 - protected mode



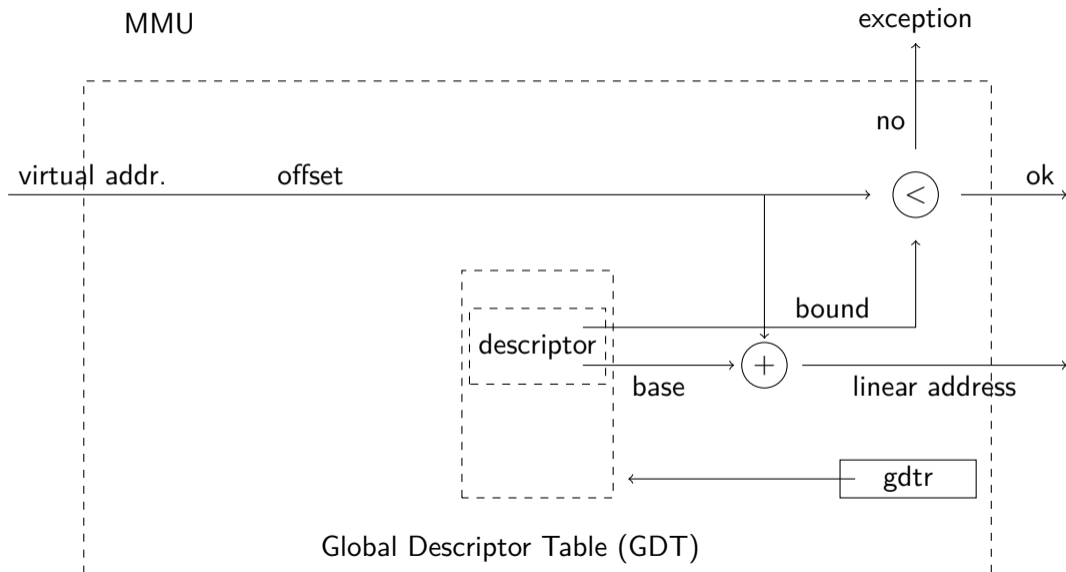
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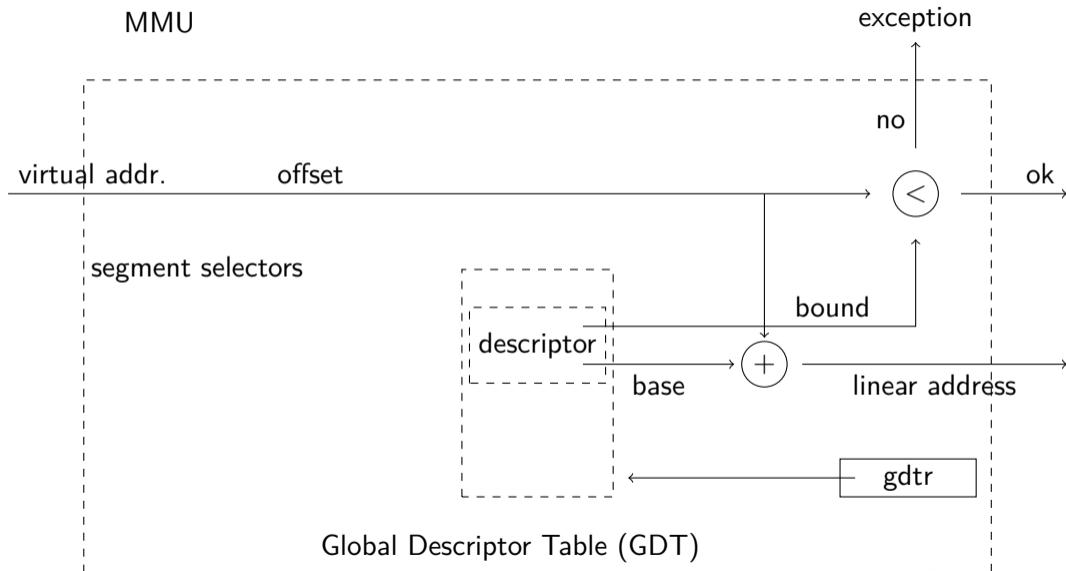
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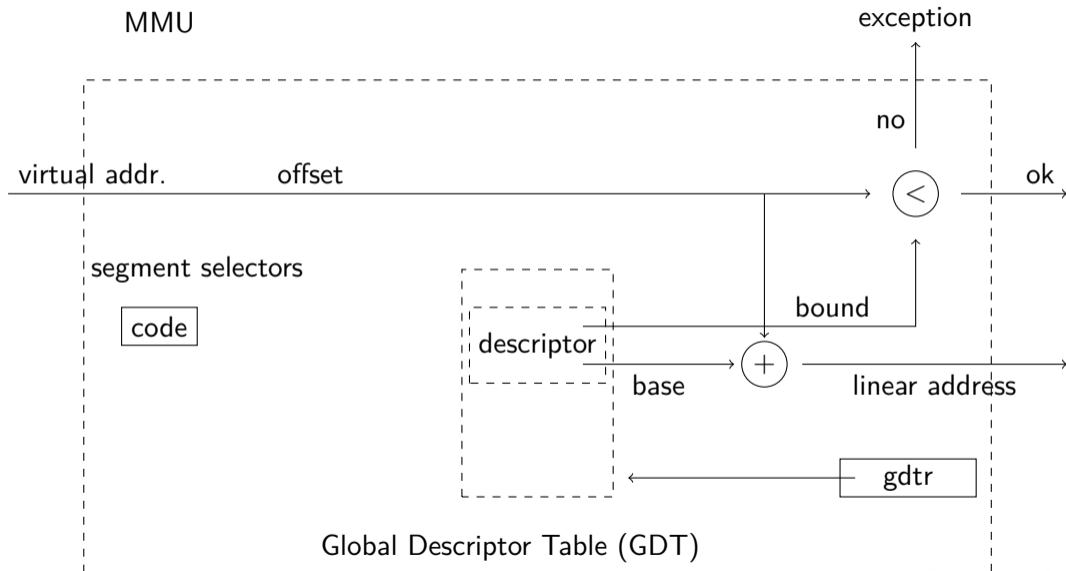
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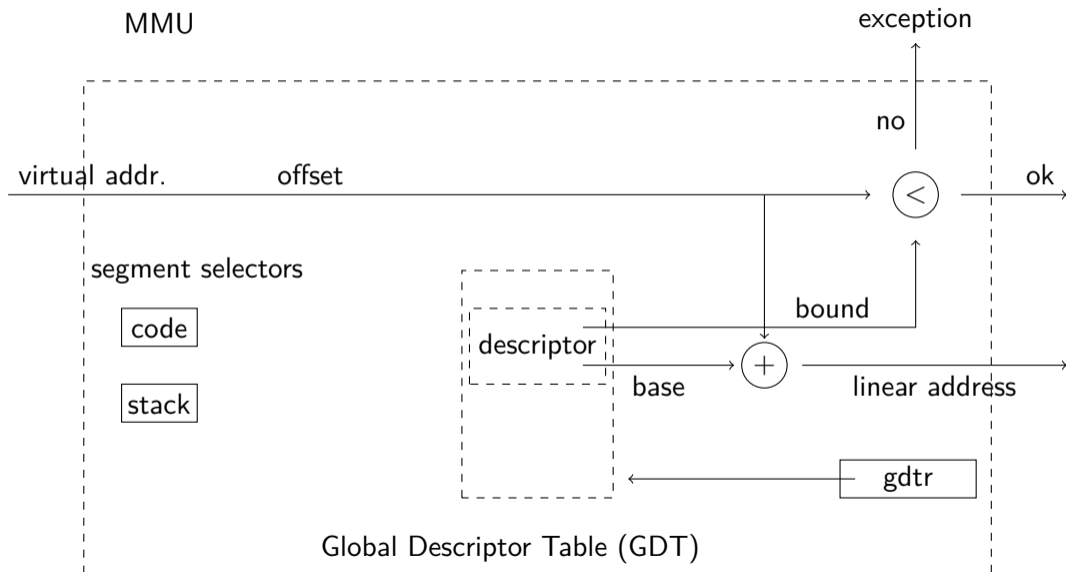
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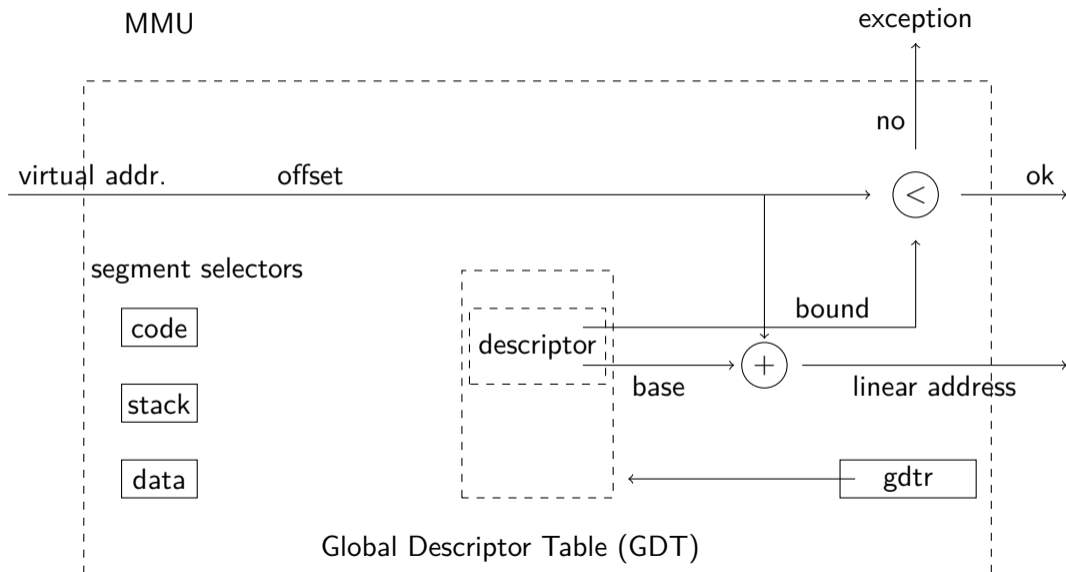
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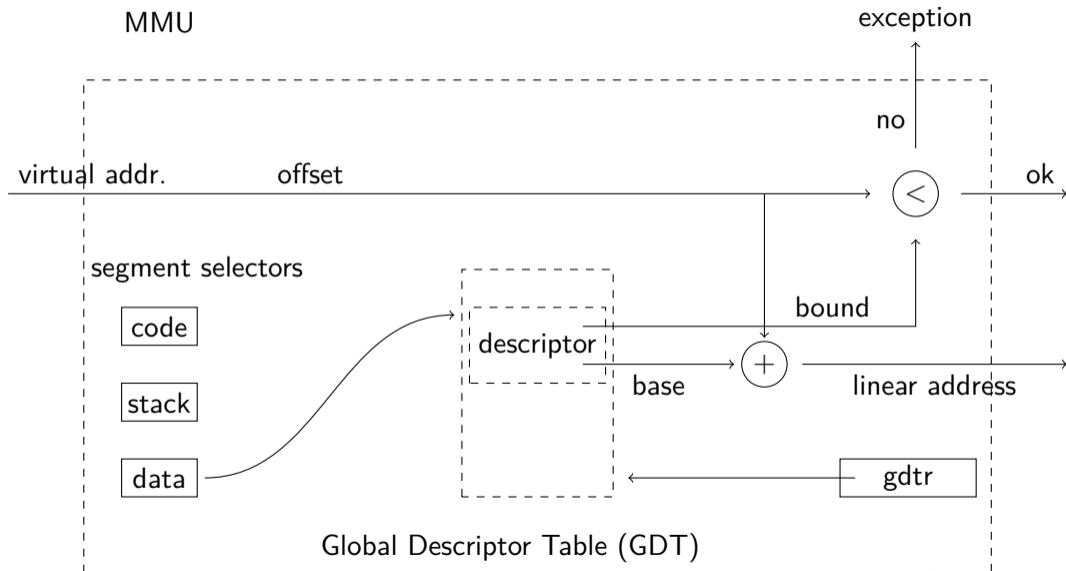
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- Segmentation is still used to refere to memory that belongs to a *specific core* or to *thread specific memory*.

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Cliffhanger - paging, the solution.