NoC System Generator
A tool for fast prototyping of multi-core systems on FPGAs

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Motivation: Embedded systems modeling

- Embedded systems are getting very complex
- We want to **abstract**, **reduce details** in the system **model**

We want **System Design Automation** to automatically add details
- it implements the embedded application on **multi-processor** platforms
- the automated synthesis of the whole system must be **fast**
Motivation: Embedded system architecture

- Embedded *architectures* are getting very complex
- *details* are increasing!

- **sea-of-cores / processors**
- NoC-based MPSoC
The problem(s)

- Huge abstraction gap
  - How to automate (and speed up) the process?
- Huge design space
  - How to explore it?
- Platform:
  - How to program it?
  - How to instantiate it?

Filling the gap through design automation: benefits

- Reduces time to market, reduces errors, reduces designer’s effort...
Proposed solution: the NoC System Generator tool

The NoC System Generator generates a complete multi-core/processor system targeted for FPGA solutions from high-level description of the application and the platform.

- An intuitive GUI permits to:
  - model the embedded system software as interconnected C processes
  - model the embedded system platform
  - explore different mapping of processes on the platform
- Processors in the platform can be selected from a range of industry accepted soft-cores, connected through a NoC:
  - NiosII, Leon3, uBlaze, HW accelerators
- Integration with Xilinx Platform Studio and Altera QSYS, permitting to target and switch between both vendors
The NoC System Generator flow

**Application model**

**Platform model**

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**NoC System Generator**

**C** + **XML**

**SW generation:**
- .c and .h files for each processor

**HW generation:**
- Altera QSYS (*.sopc, *.qsys, etc)
- Xilinx XPS (*.mhs, *.mss, etc)

**NoC .vhd files**

**XML:** HW description
- Application processes binding

**C:** SW functionality
- Processes synchronization
Results and conclusions

1. **Reduce the design time for instantiation and prototyping** of a fully configurable and heterogeneous NoC-based MPSoC.

<table>
<thead>
<tr>
<th>Target platform</th>
<th>Generate architecture model</th>
<th>Generate Xilinx/Altera project</th>
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<tbody>
<tr>
<td>4 processors</td>
<td>~100 milliseconds</td>
<td>~500 milliseconds</td>
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2. **Automatically generate HW and SW** sources and program the NoC-based MPSoC on FPGA.

3. **Explore the design space** of multiple HW and SW configurations through a intuitive GUI.

4. Support for **soft and firm real-time** systems.

More info, related papers and tutorials

https://forsyde.ict.kth.se/noc_generator/