NoC System Generator: a Tool for Fast Prototyping of Multi-Core Systems on FPGAs

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ABSTRACT

Programming and debugging of Multi-Core systems is hard. We present a Fast Prototyping tool that can generate a complete Multi-core system targeted for single-chip FPGA solutions, including software synthesis, reducing design time from weeks to a couple of hours. The system is NoC-based and configured using an XML-file. By selecting the number and type of processors for each node, both homo- and heterogeneous systems can be specified. Switching from Altera to Xilinx is done automatically.

1. INTRODUCTION

The number of cores/processors in a modern Multiprocessor System on Chip (MPSoC) is doubling every 18 months [1]. We are approaching what we call the Sea-of-Cores/Processors era [2]. MPSoC platforms are also becoming increasingly more heterogeneous, and are shifting towards communication methodologies based on Network on Chip (NoC). As the system complexity grows, the problem emerges as how to instantiate, program and explore such NoC-based MPSoCs.

In this demo we present the NoC System Generator [3][4], a fast prototyping tool to generate and program arbitrarily large heterogeneous multi-core platform from an XML configuration file, targeting Altera/Xilinx FPGAs. Resources can be selected from a range of industry accepted soft-cores, connected through a NoC. The tool automatically generates device drivers and application files for the resources on the platform and scripts for automatically compiling and running the system on the target FPGA, relieving the designer of error prone and time consuming work. The NoC System Generator also provides an experimental GUI to accelerate the design process, and to permit intuitive design space exploration (DSE) of multiple HW and SW configurations for the same application.

2. THE DESIGN FLOW

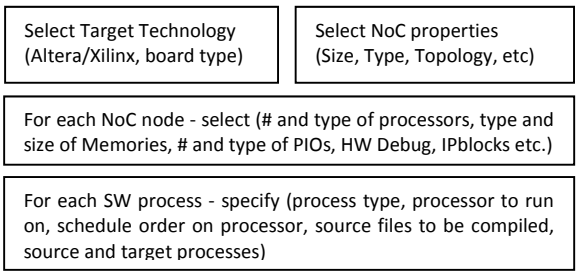

Figure 1. XML Configuration File contents

The design flow of the NoC system generator requires a high level specification of the HW architecture and the SW application, see Figure 1. Both are provided to the tool in a single XML configuration file; however we have developed a GUI which automatically generates all the input files required by the design flow. The architecture specification includes: target FPGA; NoC type and interconnection topology; the number and type of processors (Nios/uBlaze, Leon3) for each NoC node; memory size; and peripherals connected to each node. The application is modeled as a set of communicating processes, written in the C language, using a distributed memory model, using the provided communication primitives. With the GUI, the designer gets a clear representation of the underlying architecture, and can place processes on the different processors in a simple manner.

Figure 2. Hardware and Software View of a system

Figure 2 represents a 4 core architecture containing 1 process (task) for each processor. The GUI provides different types of processes to be mapped on the platform. They represent *process constructors* defining how and when communication between processes occurs. The user has only to add/describe the functionality of the processes. Communication routines are automatically created through SW synthesis, preventing the user from making errors. The NoC System Generator uses the provided specifications to generate the necessary files for implementing the system as an Altera SOPC Builder or Xilinx XPS project.

Table 1 shows the design time for the example shown in Figure 2. Once the design is running, changing the mapping of the processes or architecture configuration to explore the design space can be done easily modifying the needed parameters and followed by re-running the tool-chain. An application using this flow is described in [5].

Table 1. Design Time (Pentium M 1.4 GHz, 256MB RAM)

Specification	Generate Altera/Xilinx project	Synthesis
30 min	**1-2 seconds**	30 min

3. CONCLUSIONS AND FUTURE WORK

This demo presents the NoC System Generator [3][4], a tool for fast prototyping and design space exploration of multi-processor systems on FPGA, reducing design time from weeks to hours. Future work includes: development of algorithms for automatic DSE, extension to real time applications, extension of design entry to frameworks based on models of computation theory.

4. REFERENCES

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