




Alireza Farshin


Networked System Researcher

 kth.se/profile/farshin

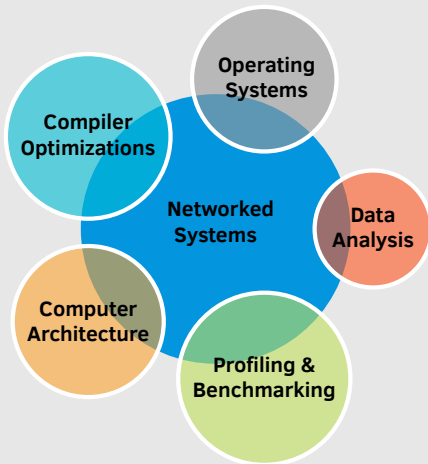
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 Google Scholar

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Technical Skills Overview



Programming & Tools

Linux • Shell Scripting • C • C++

DPDK • FastClick • Perf • LLVM

Git • Gnuplot • \LaTeX

Python • MATLAB • R

TensorFlow • Spark • Pandas

Education

PhD., Information Communication Technology

Specialization: Communication Systems

School of EECS

KTH Royal Institute of Technology

2017 - 2023 | Stockholm, Sweden

MSc., Electrical Engineering

Specialization: Digital Electronic Circuits

Amirkabir University of Technology

2015 - 2017 | Tehran, Iran

BSc., Electrical Engineering

Specialization: Electronics

Sharif University of Technology

2010 - 2015 | Tehran, Iran

Research Summary

During my doctoral studies at [KTH NSLab](#), I have improved the performance of the Network Functions Virtualization (NFV) service chains running at 100/200 Gbps by using **low-level optimization** techniques. My research has resulted in:

- [Google PhD fellowship 2021](#) award in systems and networking.
- Top systems conference papers ([EuroSys'19](#), [ATC'20](#), [ASPLOS'21](#), and [NSDI'22](#)).
- 17 patent applications filed by Ericsson (see the [published applications](#)).
- News articles at Ericsson Blog (about [memory management](#), [packet processing](#), and [packet reordering](#)), KTH news (about [CPU cache](#) and [traffic order](#)), [Tech Xplore](#), and [Framtidens Forskning](#).
- Community award at NSDI'22 for "[Packet Order Matters](#)".
- Open-source contributions ([CacheDirector](#), [DDIO-Bench](#), [PacketMill](#), [DDC-RA](#), and [IOMMU-Bench](#)).

Watch this  [video](#) and read my full  [CV](#) & [dissertation](#) for more information.

Experience

Aug 2017 - Present **Doctoral Student/Researcher**

[KTH NSLab](#)

Stockholm, Sweden

Advisors: Professor [Dejan Kostić](#) & Professor [Gerald Q. Maguire Jr.](#)

- Proposed a slice-aware memory management technique to exploit the non-uniform cache architecture (NUCA) in Intel processors and implemented [CacheDirector](#) to send packets to the right slice of the Last-Level Cache (LLC).
- Implemented a set of benchmarks ([DDIO-Bench](#)) to study the effectiveness of Data Direct I/O Technology (DDIO) at 100 Gbps.
- Implemented [PacketMill](#) to grind the whole packet processing stack and produce a customized binary for a given network function.
- Analyzed a KTH campus trace (via Spark & Pandas) to extract flow-related characteristics & predict packet interarrival time with LSTM (via Keras/TensorFlow) to reorder packets using [Reframer](#).
- Implemented a set of benchmarks ([IOMMU-Bench](#)) to study the impact of IOTLB misses on throughput and extended [Page Pool API](#) & [mlx5](#) Linux driver to use 2-MiB hugepages for packet buffers to mitigate the IOTLB wall.

Tools: DPDK, FastClick, Linux kernel, iPerf, Perf, LLVM, Intel PCM, Intel PMU Profiling Tools, Cache Allocation Technology (CAT), Spark, Pandas, Tensorflow, Gecode.

Hardware: Intel Xeon & AMD EPYC processors, NVIDIA/Mellanox & Intel NICs.

Dec 2015 - Jun 2016 **Portal Specialist**

[Mobile Telecommunication Company of Iran \(MCCI\)](#)

Tehran, Iran

Managed vendors and supervised the development of:

- eCare Application: MyMCI application for [iOS](#) and [Android](#)
- eSales Website [eVoucher](#)

Fall 2013

Co-founder and CEO

[CafeYab](#)

Tehran, Iran

Designed & implemented an application for [iOS](#) and [Android](#) for finding nearby coffee shops.

Jun 2013 - Sep 2013

Summer Intern

[Informatics Services Corporation \(ISC\)](#)

Tehran, Iran

- Ported an RF unit controller from PIC-16F877A to AtMega64A and tested the new module.
- Designed a remote-control system with HM-T and HM-R FSK modules.