Embedded Calibration of Integrated RF Frontend Blocks

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***Abstract*— Parameter variability due to process, voltage, and temperature variations (PVT) in the contemporary submicron CMOS chips makes RF circuit design risky unless proper calibration procedures are applied. They usually require careful on-chip measurements by RF sensors that can be used to compensate for the possible impairments in specs such as gain or gain mismatch which is critical e.g. in IQ setups or multi-path MIMO systems. As the sensors are exposed to the same variations as the actual RF circuitry they need to be calibrated first. In this paper the focus is on a calibration technique suitable for embedded RF sensors. This technique is based on DC measurements and statistical multivariate regression which enable mapping of the sensor DC characteristics into RF characteristics. The external RF measurements are restricted to the statistical training process preceding the actual calibration. The results obtained by simulation demonstrate reduction of output signal variations among sensors from 50% to 5% for moderate signal level and from 25% to 2.5% at full range.**

***Index Terms*—embedded RF calibration, RF sensors, RF gain mismatch**

I. Introduction

Due to process variations, RF chips manufactured in the deep submicron CMOS technologies tend to depart from the intended specifications. During operation they can also suffer from temperature and supply voltage variations (jointly referred to as PVT). To combat those effects calibration techniques supported by DSP resources can be employed [1]–[3]. As the access to the internal nodes of RF chips is limited a dedicated built-in calibration circuitry is necessary. The common variations in RF gain or mismatch can usually be tracked by embedded RF sensors (detectors) converting RF signal into a proportional DC voltage [4]–[7]. Such a scenario applies in particular to transmitter RF stages where IQ gain mismatch or imbalance in MIMO paths is of utmost importance [8],[9]. Based on those measurements the necessary gain corrections can be conveniently carried out at the transmitter baseband. Clearly, the RF sensors and the supporting measurement circuitry undergo similar PVT variations as the RF circuit under calibration so they need to be calibrated first.

In this paper a calibration technique for embedded RF sensors is presented. It is based on internal DC measurements and statistical mapping of DC characteristics into RF characteristics which serve the actual RF measurements. As compared to the previous work [10], here a complete calibration setup including DAC, MUX, and ADC is considered. Using this model also a scenario with distributed RF sensors can be covered provided they are manufactured in one process so that one statistical measure applies to them. This case reflects in particular a MIMO system with multiple power amplifiers each provided with a separate RF sensor.

In the following the paper presents the calibration setup, and the calibration procedure. The results for a Monte-Carlo model of the RF sensor with DAC, MUX, and ADC designed in 65 nm CMOS demonstrate calibration errors (variation in measurements by different detectors) of 2.5% for a full range signal and < 5% for 6 dB back-off.

II. Calibration Set-up

The calibration circuitry for a set of RF sensors (A to F) is presented in Fig. 1. For measurements the sensors are connected to nodes of the RF frontend blocks under calibration (not shown here). Loading effects are avoided due to high input impedance of the sensors (5 kΩ at 2 GHz). Their outputs (DC) are connected to T-ADC through a MUX and a DC bus. For calibration of the sensors an internal DC signal is applied from T-DAC and the corresponding output signals are measured by the same T-ADC. Additionally, one sensor (A) can be accessed from outside of the chip. An RF calibration signal can be applied to this sensor for comparison of the sensor response with the response to internal DC input. A measurement like this, carried out on a sample of chips, allows to identify a mapping between DC-DC and RF-DC characteristics of the RF sensors. The derived mapping is used for all sensors, (esp. B to F) which cannot be accessed from outside because of layout limitations at RF frequencies in GHz range. To calibrate a sensor it is sufficient to measure its DC-DC characteristics and next make use of the derived mapping. Importantly, in this setup calibrated is the complete path from the sensor input to the ADC output. The DC signal accuracy is limited that contributes to the absolute calibration error but the relative calibration error is not affected since DAC is shared by all sensors.

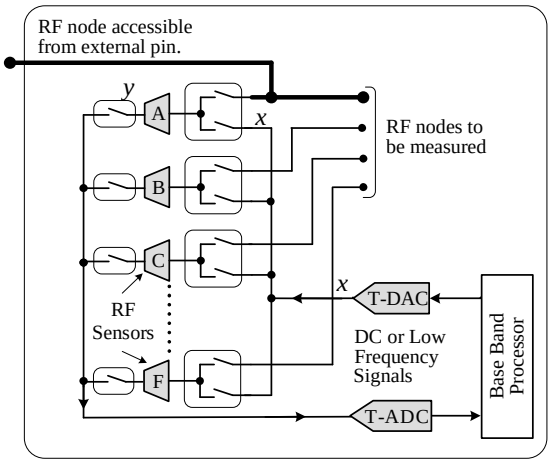

Figure 1. Architecture of calibration circuitry.

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III. Circuit Design

The calibration circuit was designed using 65 nm CMOS standard process. Assuming 1% calibration accuracy the required resolution of T-ADC and T-DAC can be estimated as 9 bit.

Since T-DAC serves as the reference DC source in the calibration it is the most challenging part of the project. It was designed as a differential binary-weighted current steering 10-bit DAC with digital background LMS calibration [11]. In Monte-Carlo simulation with 3σ spread in the device parameters it has shown the worst case INL and DNL to be within 6 LSB that appeared sufficient compared to the statistical errors with an ideal DAC.

The T-ADC was designed as single-ended SAR converter owing to its simplicity and low silicon overhead. Compensation of offset in the comparator was assumed. The worst case DNL and INL over process and mismatch variations with 3σ spread in device parameters for the T-ADC were 11 LSB and 9 LSB, respectively, corresponding to approx. 1% output variation.

The multiplexer and demultiplexer were realized as transmission gate switches. Since the input impedance of the RF detector and T-ADC is very high, the transmission gate on-resistance does not have any measurable effect on the performance of the calibration chain. The RF sensor was designed as a differential circuit [10] with minimum size devices to achieve possibly high input impedance (5 kHz at 2 GHz).

IV. Calibration Procedure and Results

The typical sensor characteristics are illustrated in Fig. 2. By modeling them with two polynomials the task is to map one set of coefficients (a_{DC}) into the other (a_{RF}). As the both sets are characterized statistically the mapping is derived by a regression technique using the neural network (ANN) implemented as the multilayer perceptron (MLP) with two hidden layers. To verify this approach data from Monte-Carlo simulation on 500 statistical samples (of complete calibration path) was collected. The data set was randomly split in two equal parts to serve as the training and validation data. After the ANN was trained to provide the wanted mapping, the validation data was applied to ANN to reconstruct the RF responses and the validation errors were calculated by comparison with the actual RF responses (Fig. 3). This result should be compared to the maximum variations in the RF responses observed before calibration as shown in Fig. 4, where the mean values are chosen as a reference. The minimum variations of approx. 25% are reduced to 2.5% represented by the validation errors.

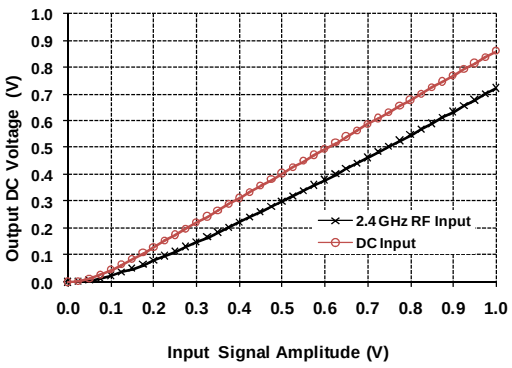

Figure 2. Typical ch-cs of RF sensors designed in 65 nm CMOS.

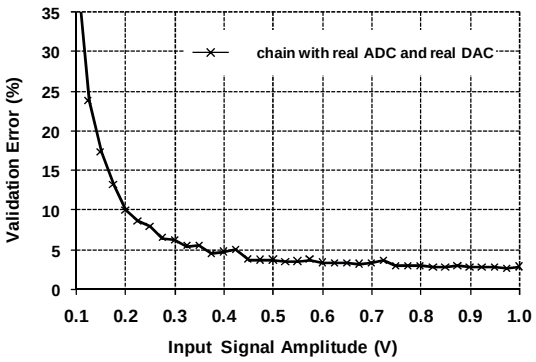

Figure 3. Validation error after calibration.

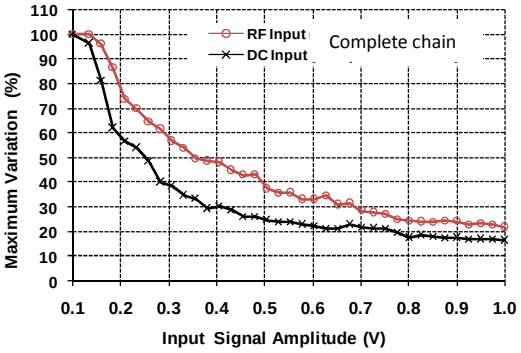

Figure 4. Maximum variations in RF responses before calibration.

V. Conclusion

The presented calibration procedure of embedded RF sensors has proven effective. The attained accuracy mainly depends on correlation between the sensor parameters for DC and RF input. The typical calibration error for the mid-range input voltage is less than 3.5 %, which is a promising result and the method could be adopted in practice. Appealing are in particular applications of this technique in multi-path MIMO systems where imbalance in gain tends to result in significant performance degradation.

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