Simulink is an industrial de-facto standard for building executable models of embedded systems at system-level. Once the Simulink system-level model has been validated through simulation, the problem arises as how to automate the generation of a working prototype from the Simulink system-level model.

In addition, the techniques enabling fast-prototyping of Simulink models should target implementations onto state of the art multi-processor systems on chip (MPSoCs).

**Contributions**

1. to automate the synthesis of a Simulink model onto a network-on-chip (NoC) based MPSoC implemented on FPGA;
2. to constrain the Simulink model and its MPSoC implementation to share a common semantics domain;
3. to propose a generic method based on the established model of computation (MoC) theory;

**Platform-based Design Flow**

1. Simulink Embedded Coder
2. Extraction of rt_onestep function(s)
3. System-level specification
4. HW/SW compilation
5. Prototype synthesis on FPGA

**XML Platform Description**

```xml
<root name="Cosummit_2x2">
  <parameter name="targetArchitecture" value="System"/>
  <parameter name="targetFramework" value="Simulink"/>
  <parameter name="boardType" value="DE2-115"/>
  <parameter name="targetManufacturer" value="Altera"/>
  <parameter name="targetDirectory" value="./generated_files/"/>
  ...
</root>
```

**HB Wrapper**

```c
int main(void)
{
  // Wait for first GlobalSync
  while(GlobalSync==0)
  {
    p0_init();
  }
  // Clear Synchronization Flag
  NOC_RNI_CLEAR_SYNC_FLAG();
  ...
  return 0;
}
```

**HB Compliant MPSoC**

**References**


**Future Work**

- Extend wrappers to other MoCs
- Automatic generation of XML file from system-level model through Design Space Exploration

**Tool Features**

- Prototype heterogeneous NoC-based systems for Xilinx and Altera FPGAs - Nios2, Leon3, uBlaze, custom HW
- Design and prototype generation time heavily reduced
- Targets low cost FPGAs (low memory and low logic elements availability)
- Easy integration with commercial tools for FPGA development (Altera QSYS and Xilinx Platform Studio)

**Design Flow Steps**

1. System-level model with Simulink; Simulation of the system; Embedded Coder: C code generation;
2. XML description of the target platform; NoC System Generator:
   - generation of platform HDL;
   - generation of process wrappers;
3. Extraction of rt_onestep function from the Embedded Coder generated C files; Embed the "clean" rt_onestep function in the process wrapper (HB wrapper), scheduling its execution on the HB ticks;
4. Compilation of the HDL for FPGA; Compilation of the C code for each PE;
5. Configure the FPGA; Download and run the compiled SW for each PE; Collect the prototype results;